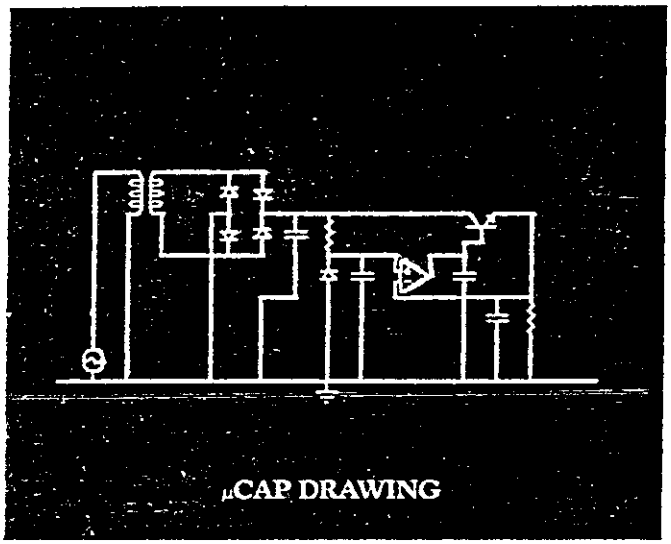
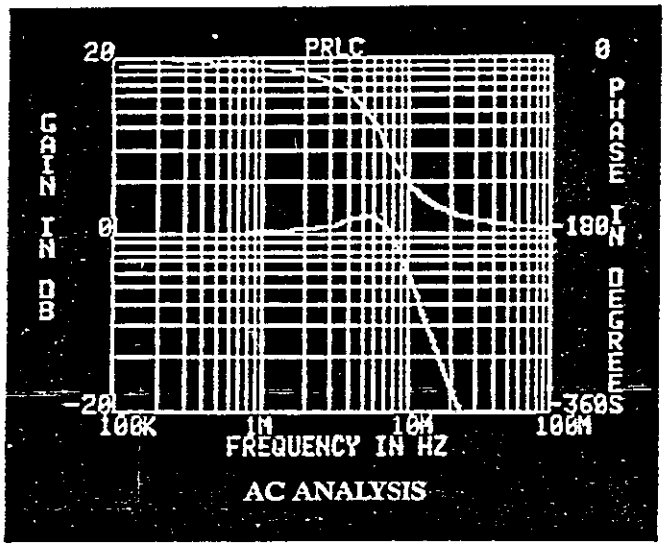
Modello del transistor pessimo.

μCAP

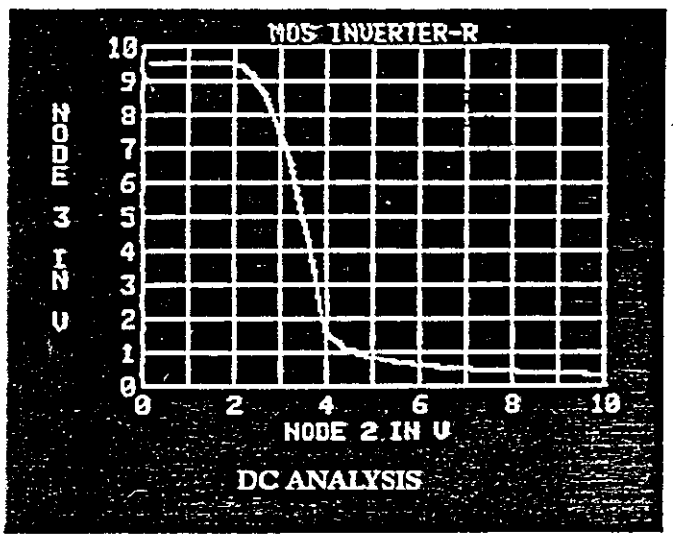
MICROCOMPUTER CIRCUIT ANALYSIS PROGRAM



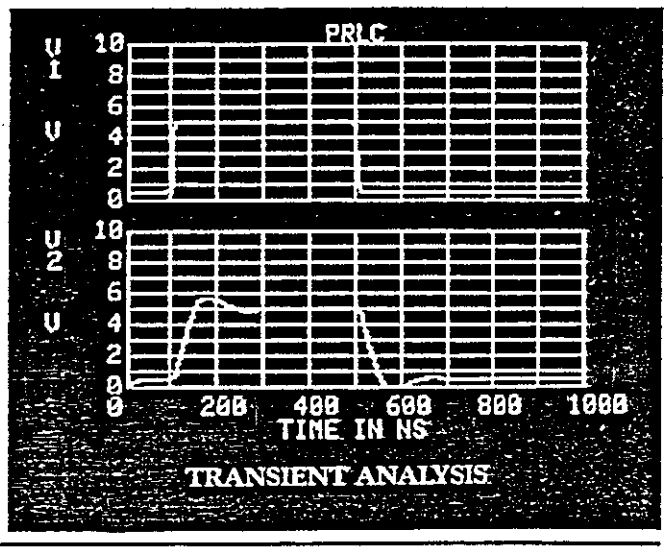
μCAP DRAWING



AC ANALYSIS



DC ANALYSIS



TRANSIENT ANALYSIS

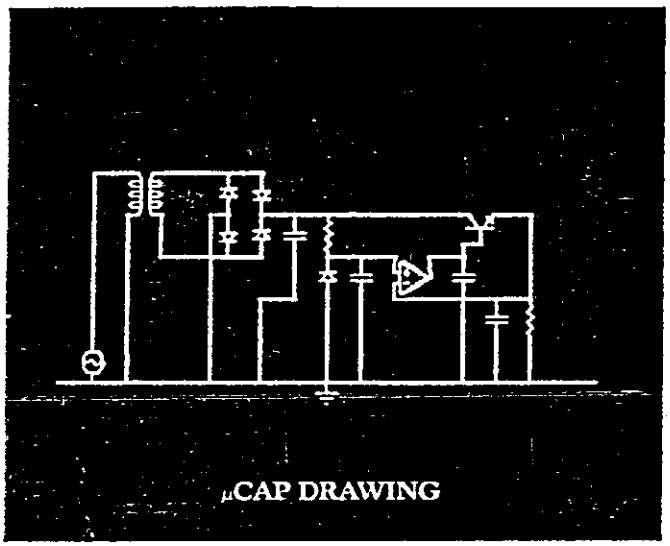
SPECTRUM

Professional Software Products

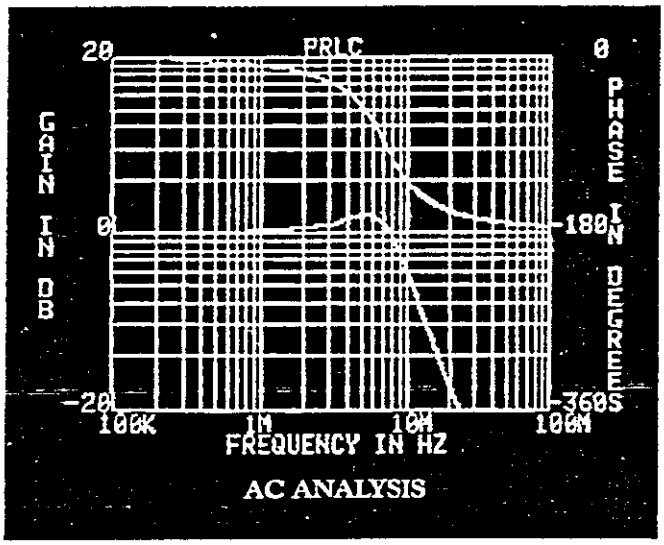
Modello del transistor pessimo.

μCAP

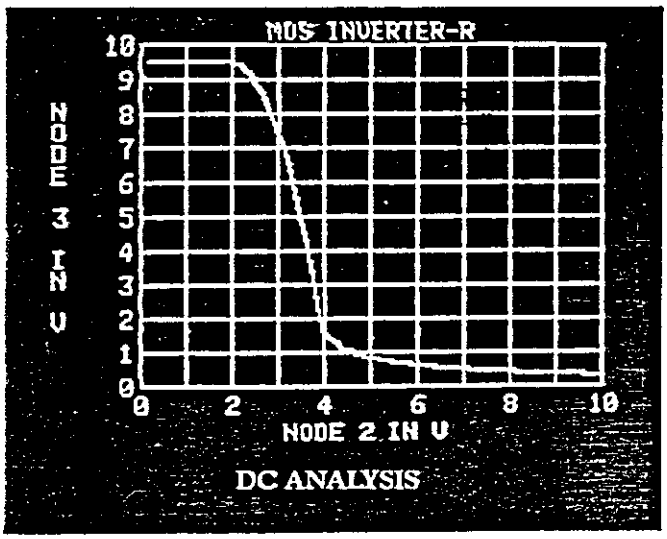
MICROCOMPUTER CIRCUIT ANALYSIS PROGRAM



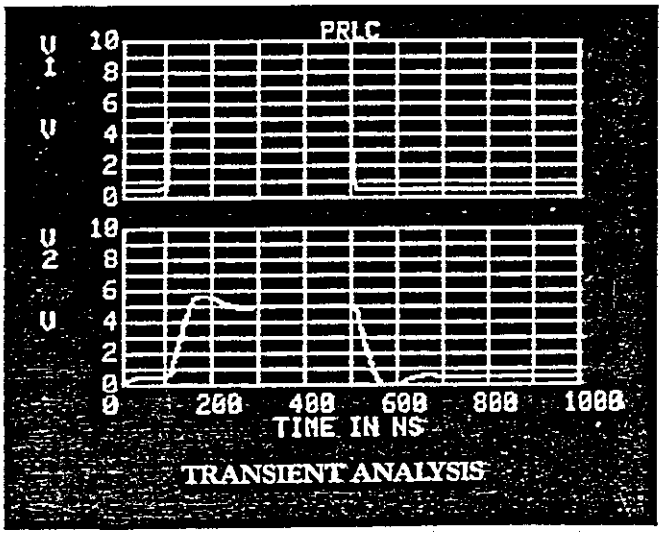
μCAP DRAWING



AC ANALYSIS



DC ANALYSIS



TRANSIENT ANALYSIS

SPECTRUM

Professional Software Products

SPECTRUM
SOFTWARE 690 W. FREMONT AVE., SUITE 11 SUNNYVALE, CA 94087 PHONE: 408-738

MICRO-CAP

MICROCOMPUTER CIRCUIT ANALYSIS PROGRAM

COPYRIGHT 1982

SPECTRUM SOFTWARE

BY

ANDREW V. THOMPSON

MICRO-CAP
MICROCOMPUTER CIRCUIT ANALYSIS PROGRAM
TABLE OF CONTENTS

		PAGE
I	INTRODUCTION	
	• Getting Started-APPLE II	1-2
	• Getting Started-IBM PC	1-5
	• Overall Program Flow	1-8
	• Component Types	1-10
	• An Easy Example	1-11
II	THE DESIGNER MODULE	
	• Main Menu	2-1
	• The Drawing Board	2-2
	• Command Menu	2-3
	• Component Types	2-5
	• Orientation Definition	2-6
	• Adding and Removing Shorts	2-7
	• Clearing the Screen	2-7
	• Retrieving Old Circuit Files	2-8
	• General Guidelines	2-8
	• Command Practice	2-9
	• Error Messages	2-13
III	THE ANALYZER MODULE	
	• Main Menu	3-1
	• Saving/Retrieving/Deleting Network Files	3-2
	• Creating/Reviewing/Editing Networks	3-3
	• Standard Component Editor	3-11
	• Sample Standard Components Library	3-14
	• Generating User-Defined Sources	3-15
	• Creating New Data Disks	3-18
IV	TRANSIENT ANALYSIS	
	• Prologue	4-1
	• Monitoring Current, Power and Energy	4-4
	• Resetting Circuit Variables	4-5
	• Setting Initial Conditions	4-6
	• Waveform Dump Option	4-7
	• Display Mode Selection	4-8
	• The Transient Analysis Display	4-10
	• Epilog	4-13
	• Printer Plot Example	4-14
	• Table of Voltages Example	4-15
V	AC ANALYSIS	
	• Prologue	5-1
	• AC Analysis Display	5-4
	• Printer Option	5-6
	• Epilog	5-7

TABLE OF CONTENTS
(CONT)

		PAGE
VI	DC ANALYSIS	
	• Prologue	6-1
	• DC Analysis Display	6-2
	• DC Analysis Example	6-3
	• DC Analysis Printer Option	6-5
	• DC Convergence	6-6
	• Stopping an Analysis	6-7
VII	COMPONENT MODELS	
	• Diodes	7-1
	• Bipolar Transistors	7-6
	• Opamps	7-8
	• Transformers	7-11
	• Sinusoidal Voltage Sources	7-13
	• Programmable Voltage Waveforms	7-14
	• MOS Transistors	7-15
	• Polynomial Sources	7-18
	• Resistor, Inductor & Capacitor	7-19
	• Battery or Power Supply	7-20
	• Switches	7-21
	• User Source	7-24
VIII	APPENDICES	
	• A: Maximum Specifications	A-1
	• B: Hardware Requirements	B-1
	• C: Things to Watch Out For	C-1
	• D: Liscense Agreement	D-1
	• E: Examples	E-1

GETTING STARTED-APPLE II

CONTENTS

Before you do anything else inspect the contents of your package. You should find:

1 Demo diskette
1 Data diskette
1 Program diskette
1 Protection key

The Demo Diskette is a free-running demonstration of MICRO-CAP capabilities. To see it in operation simply turn on your computer, put the disk in drive #1 and watch! Do that now before you proceed.

MICRO-CAP is supplied with a primary program disk in copyable format.

MICRO-CAP is also supplied with a data diskette. Contained on the disk are several sample circuit files. The diagrams for these circuits are shown in the Appendices. They are provided as guides to facilitate your learning of MICRO-CAP. The data diskette also contains a Library file of Standard Components. The file name is STANDARDS. Whenever you make a new data diskette you will need this file so do not discard or otherwise damage it as it will be used to "clone" a new data diskette.

REQUIRED HARDWARE

The next step is to check your system to see if it has the required hardware. You need:

1. An APPLE II with Applesoft in ROM on the motherboard or an APPLE II Plus or an APPLE II-e. The program will not run on an APPLE III even under emulation mode.

2. A 16K RAM card (or language card) installed in slot 0 (not necessary with an APPLE II-e).

3. Two Disk Drives (DOS 3.3).

4. A Monitor.

5. Optional printer with parallel printer interface card (MICRO-CAP will work with some serial interface boards but it is not guaranteed to work with all such boards).

GETTING STARTED-APPLE II

PROTECTION KEY

The Protection Key must be installed to run MICRO-CAP. It is not required to run the demo diskette. The key is installed in the game socket in exactly the same way as the APPLE game paddles. Follow the instructions contained in the packet. Do this before proceeding.

MAKING BACKUPS

All MICRO-CAP diskettes are provided in Standard DOS 3.3 format. Making backup copies is thus accomplished by using either the COPYA or COPY program on your DOS 3.3 System Master diskette. Do not use any of the NIBBLE copiers as these tend to produce less reliable copies that the Standard APPLE II copy programs.

We suggest that you make a backup copy of both the program and data diskettes and then put the originals in a safe place. The backup copies will then become your "working copies".

WRITE-PROTECT TABS

Remove all write-protect tabs from your working copy and from the data diskette. MICRO-CAP uses the program diskette to store buffer files and must not be write-protected. All user data files are contained on the data diskette and only there. Consequently, you may wish to create backup copies of your data diskette from time to time.

GETTING STARTED-APPLE II

CHECKLIST

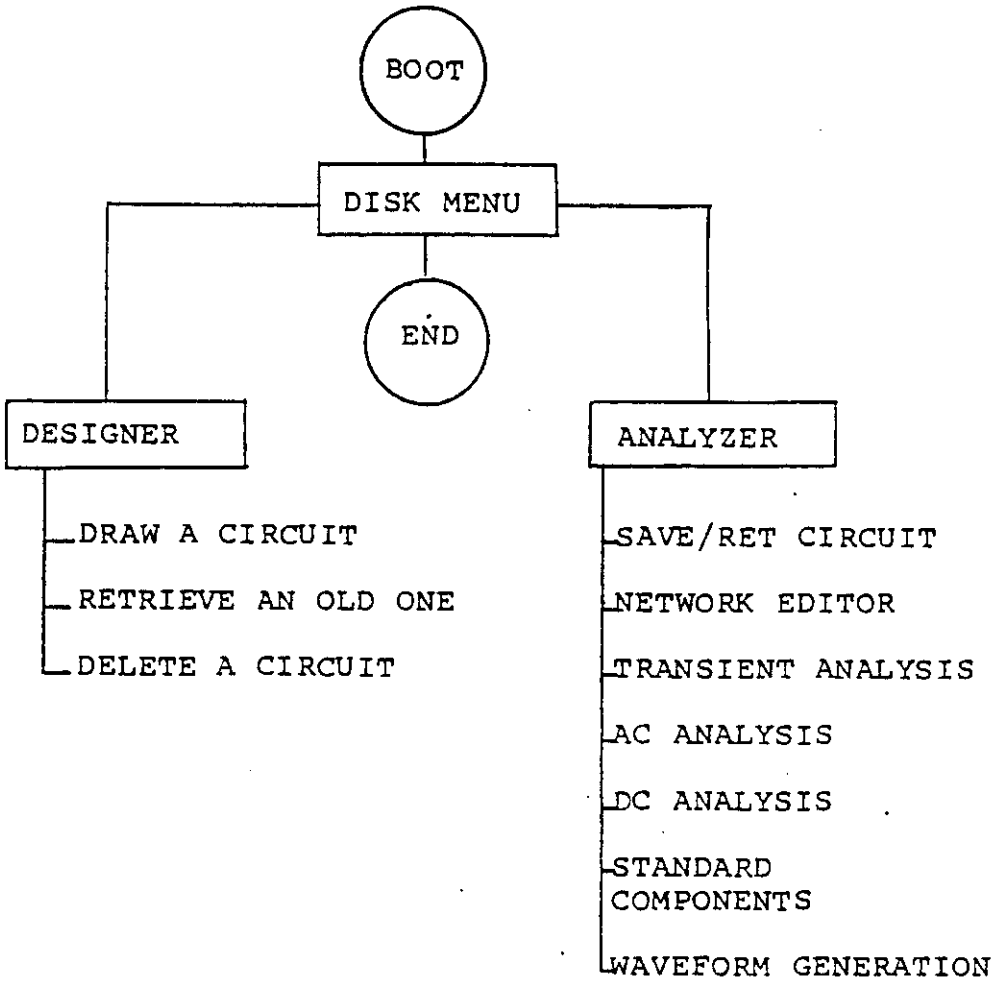
Before you start make certain that you have:

1. Inspected and verified the package contents.
2. Checked that your system has the necessary hardware.
3. Ran the Demo Diskette.
4. Made backup copies of the program and data diskettes.
5. Installed the Protection Key.
6. Removed all write-protect tabs from working copies.

If you have missed anything go back and do it now. Otherwise you're ready to start. Place the program diskette in drive #1 and the data diskette in drive #2. Turn on the computer and you are ready to go. Before we actually begin, let's review the overall program structure. Turn to page 1-8 to proceed.

OVERALL PROGRAM FLOW

A simplified program flow diagram is shown below.



When you boot the program disk the first program that comes up is the DISK MENU. This small program allows you to select:

1. The Designer Module
2. The Analyzer Module
3. End

If your system is an IBM then this program will first remind you to press the CAPS-LOCK key.

OVERALL PROGRAM FLOW

To draw your circuit you select the 1: DESIGNER option. This loads and runs the DESIGNER module. It allows you to draw new circuit diagrams, retrieve old ones from the data diskette and create hard copy printed images of the diagram.

To analyze your circuit you select 2: ANALYZER from the DISK MENU. This loads and runs the ANALYZER module. This module enables you to:

1. Save and retrieve circuit files created by the DESIGNER.
2. Edit them if you wish.
3. Printout Netlist descriptions of your circuit.
4. Run AC, DC, or Transient Analysis.
5. Review/edit your Standard Component model parameters.
6. Generate user-defined waveforms.

COMPONENT TYPES

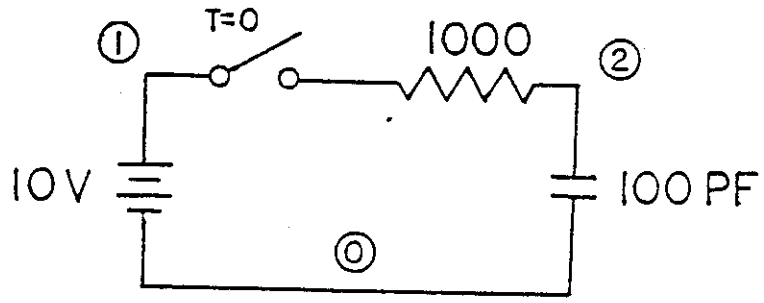
MICRO-CAP allows networks to consist of the following types of components. Components in the left column are specified with a single parametric value (such as 1000). Components in the right column are called Standard Components and are specified by a type number.

Networks may contain up to the maximum number (shown in parentheses) of each component.

PARAMETRIC TYPES		STANDARD TYPES	
BATTERIES	(10)	DIODES	(20)
RESISTORS	(60)	BIPOLAR TRANSISTORS	(20)
CAPACITORS	(60)	TRANSFORMERS	(10)
INDUCTORS	(40)	MOS DEVICES	(20)
USER SOURCES	(1)	OPAMPS	(20)
SWITCHES	(10)	SINUSOIDAL VOLTAGE SOURCES	(5)
		PROGRAMMABLE VOLTAGE SOURCES	(5)
		POLYNOMIAL SOURCES	(10)

AN EASY EXAMPLE

Before we go into the detailed operation of MICRO-CAP let's illustrate how to use it with an easy example. The example we will use is a simple battery/resistor/capacitor circuit which we will call BRC. Note that the node numbers have been labelled sequentially from 0 up to 2. Zero is always used for ground and no node numbers have been skipped.



Place the program disk in the primary drive (A for IBM), 1 for APPLE) and the data diskette in the secondary drive (B for IBM, 2 for APPLE). Boot the system (PR#6 for Apple, CRTL/ALT/DEL for IBM). If your system is an IBM you will have to press the CAPS lock key and then press the (RETURN) key.

When the DISK MENU comes up on the screen, select the Designer Module by pressing 1. When the DESIGNER menu comes up on the screen select 1: START A NEW CIRCUIT DIAGRAM. At this point the program will clear the screen, display the command menu and await your command.

AN EASY EXAMPLE

The commands we will be using here are:

KEY	COMMAND
I	CURSOR UP
J	CURSOR LEFT
K	CURSOR RIGHT
M	CURSOR DOWN
A	ADD A COMPONENT
Q	QUIT

The cursor is the flashing box in the middle of your display. When anything is drawn it originates at the cursor. To illustrate, press the "M" key 5 times and the cursor will move down to the ground line.

Now press "A". The system will request:

ENTER TYPE OF COMPONENT.

Type in BAT (for BATTERY), then (RETURN). The system will then request:

DIRECTION (R, L, U, D)?

Press "U" (for UP). The system then requests:

PARAMETER?

Type in 10 (for 10 volts), then (RETURN).

The system then draws a battery, sets its value to 10 volts and moves the cursor to the opposite end of the battery (anticipating your desire to continue drawing from there).

Next we will add the resistor. The following key strokes will accomplish it:

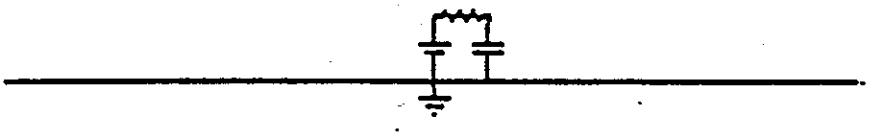
1)	A	(no RETURN)
2)	RES	(RETURN)
3)	R	(no RETURN)
4)	1000	(RETURN)

AN EASY EXAMPLE

Next add the capacitor with these entries:

1)	A	(no RETURN)
2)	CAP	(RETURN)
3)	D	(no RETURN)
4)	1E-10	(RETURN)

With this last step the circuit diagram should look like this on the display screen.



Now press Q (no RETURN). If your system is an APPLE select 1 from the Epilog menu.

The system will then print the message:

HIT RETURN TO SAVE THIS CIRCUIT UNDER
THE FILE NAME XXXXX

OR ENTER A NEW FILE NAME ?.....

Type in BRC (RETURN). The system will then file the BRC circuit. If your system is an APPLE select 5 from the Epilog menu to return to the Designer Main Menu. From here press 4 to return to the DISK MENU. From the DISK MENU select 2: RUN ANALYZER MODULE.

From the ANALYZER main menu select item 1. The system will print the query:

SAVE (S), RETRIEVE (R), OR DELETE (D) A
NETWORK FILE?

Press R and the system will ask if you wish a catalog.
Press N and the system will print the message:

PRESS RETURN TO SELECT THE FILE NAME BRC

OR ENTER A NEW NAME?

Just press (RETURN) and the program will read in the BRC file and return to the ANALYZER menu. From here select 2: REVIEW/CREATE/EDIT NETWORKS and the system will show the Network Editor form displaying our circuit BRC. It should look like this:

NETLIST :
BRC CIRCUIT

REF	COMPONENT	CONNECTIONS				PARAMETER
		IN		OUT		OR
NO.	NAME	-	+	-	+	TYPE
1:	BATTERY	0	1	0	0	10
2:	RESISTOR	1	2	0	0	1000
3:	CAPACITOR	2	0	0	0	1E-10

UP DOWN ADD EDIT REMOVE PRINTER QUIT

Line numbers 1-3 show the list of components (called a Netlist) that has been generated by the DESIGNER module for our circuit BRC.

Now press Q and the system returns to the ANALYZER menu. From here select 3: TRANSIENT ANALYSIS. The system will now load and run the module used for transient analysis. That module begins with a prologue during which the user enters the various simulation limits to be used. Type in the following values:

SYSTEM PROMPT	YOUR ENTRY
MAXIMUM SIM TIME (SEC)	1E-6
MAXIMUM DELTA T (SEC)	1E-8
MINIMUM ACCURACY (%)	5
UPPER TRACE NODE(S)	1
OFFSET FOR #1	0
SCALE FACTOR FOR #1	1
LOWER TRACE NODE(S)	2
OFFSET FOR #2	0
SCALE FACTOR FROM #2	1

This set of entries tells the system to run a simulation from T=0 to T=1E-6 (1 micro-second) using maximum time increments of 1E-8 (10ns) and to display the waveforms on nodes 1 and 2 each with a scale factor of 1V/DIV and zero offset voltage. Following the last entry the system will ask:

ARE THESE CORRECT (Y/N)?

to which you respond "Y". The system then asks:

ZERO INITIAL CONDITIONS (Y/N)?

Respond with "N".

The system then presents the Initial Conditions Option.

Respond with "3" to bypass this option for now.

The system will next request:

DUMP NODE WAVEFORM TO USER FILE (Y/N)?

Respond with "N".

Finally the system will request:

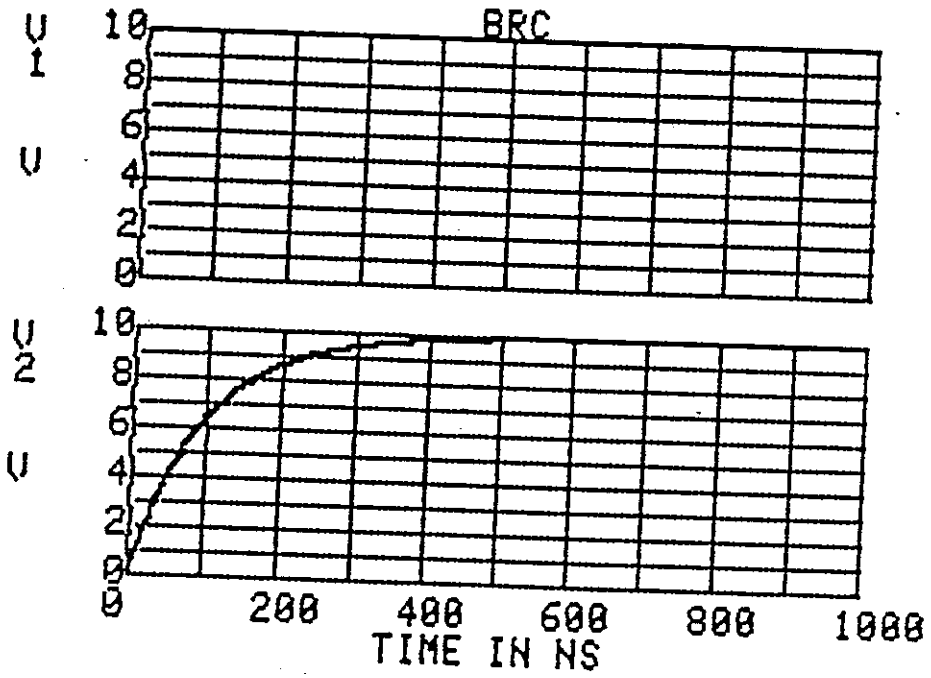
SELECT DISPLAY MODE

1. CRT DISPLAY
2. PRINTER PLOT
3. TABLE OF VOLTAGES

ENTER YOUR CHOICE

Respond by pressing 1.

The system then creates the Transient Analysis Waveform Display and runs the actual simulation routines. A complete simulation for the BRC circuit would look like this:



AN EASY EXAMPLE

In the top section is shown the waveform for node 1, the battery. It is, of course, constantly at 10V. In the bottom section is shown the waveform for node 2, the capacitor/resistor junction. As expected the voltage is rising exponentially from 0 volts to a final voltage of 10 volts. The time constant of the exponential is 100ns, exactly what is expected from the resistor and capacitor values.

$$TC = R \times C$$

$$TC = 1000 \times 10^{-10} = 100ns$$

Following completion of the simulation, the message:

PRESS ANY KEY

appears at the bottom of the screen (APPLE ONLY). Press any key and the system will respond with the Epilog menu. Press 4 to return to the Analyzer menu.

AN EASY EXAMPLE

Now let's run an A/C analysis on the same BRC circuit. Assuming that you are now at the ANALYZER main menu, retrieve the BRC file exactly as before using option 1. Then select option 4: FREQUENCY DOMAIN (AC) ANALYSIS from the menu. In this mode of analysis all AC voltage sources are left out of the circuit for purposes of the analysis. All batteries and inductors are replaced by .001 ohm resistors.

As before the system will load and run the prologue first to establish the analysis limits. Since we know our circuit has a time constant of 10-7, the frequency range of interest will be 100KHZ to 100 MHZ, so let's use these as limits.

Enter the following response:

QUERY	YOUR RESPONSE
LOWEST FREQUENCY	1E5
HIGHEST FREQUENCY	1E8
LOWEST GAIN	.01
HIGHEST GAIN	1
INPUT NODE NUMBER	1
OUTPUT NODE NUMBER	2
MIN ACCURACY (%)	5
HIGHEST PHASE SHIFT	0
LOWEST PHASE SHIFT	-90

AN EASY EXAMPLE

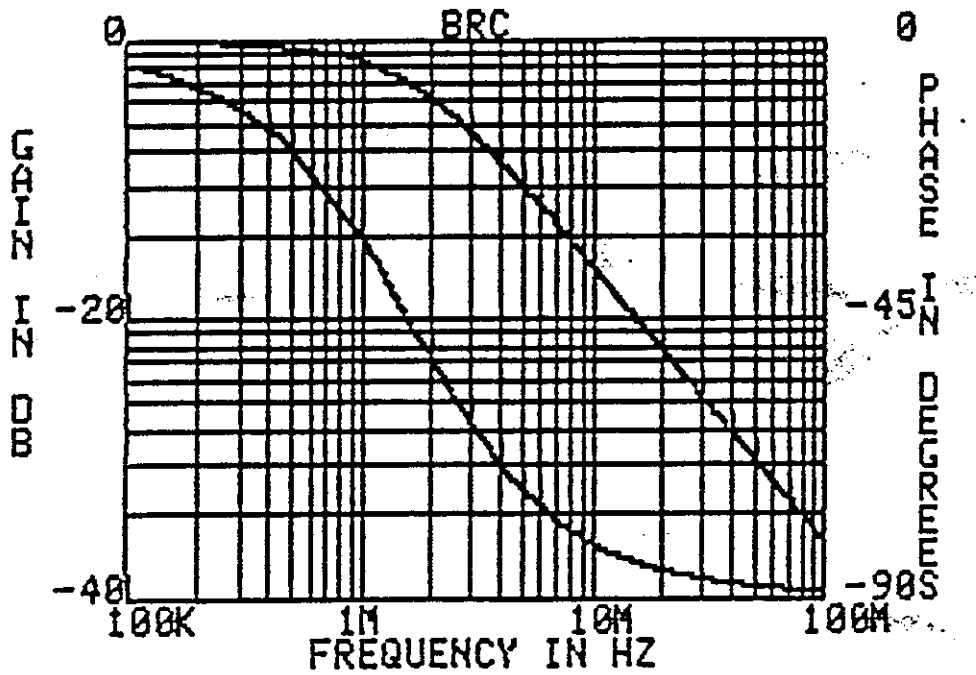
Respond "Y" to the query:

ARE THESE CORRECT (Y/N)?

Respond as follows to the querys:

INCLUDE MINOR GRIDS	Y
GRID DOT SPACING	2
HARD COPY (Y/N)	N

the system will then create a Bode plot showing the GAIN and PHASE shift from node 1 to node 2 in our BRC circuit. It should look something like this:



Press any key and the system will display the Epilog menu. Press 4 to return to the Analyzer main menu.

That completes our short example. Though there is much left to review, by now you should have a basic understanding of how circuits are drawn, listed and analyzed. The suceeding chapters will go into detail as to how each major module functions and how to deal with more complex circuits and analysis requirements.

II THE DESIGNER MODULE

As the name implies this module is used to design (eg. draw) your circuits. It's principal function is to enable the user to literally draw circuit diagrams on the video display using the graphics commands. Circuit files may be saved, retrieved, edited and refiled under as many different names as you like.

It is important to remember that each circuit diagram saved uses 8% to 13% of the total storage on the data disk. This means that 7 to 12 circuit diagrams are the most that can be filed on any one data diskette. Of course, there is no limit to the number of data diskettes that you can use. The program does not check to see if adequate space exists before filing but does recover in case there is insufficient room to store your current circuit diagram.

Additional data disks can be created by simply initializing a disk. For APPLE this means performing an INIT command. For IBM this means performing a FORMAT command. The only file that need be on the data disk before using it is the Standards file. The procedure for placing this file on new data disks is discussed in the ANALYZER section of this manual.

The main menu of the DESIGNER module provides these options:

MICROCOMPUTER CIRCUIT ANALYSIS PROGRAM

DESIGNER MODULE

1:START A NEW CIRCUIT DIAGRAM

2:RETRIEVE A CIRCUIT FROM DISK

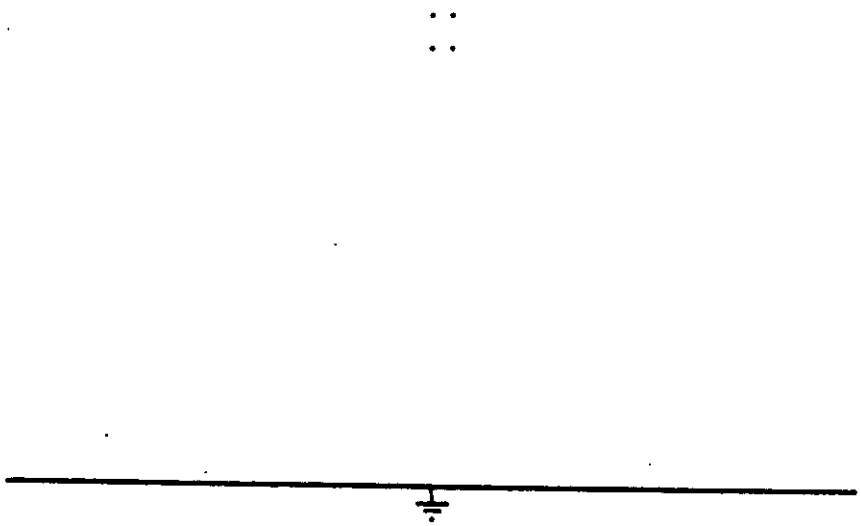
3:DELETE CIRCUIT FILE FROM DISK

4:RETURN TO DISK MENU

Option 1 is used to start drawing a new diagram. Option 2 is used to retrieve a diagram from your data disk. Option 3 is used to delete a circuit file from your data disk. Option 4 simply returns control to the DISK MENU.

THE DRAWING BOARD

Select Option 1 and the program will prepare the drawing board. It looks like this:



```
I:UP     M:DOWN        J:LEFT      K:RIGHT
S:SHORT  B:BEGIN LINE  E:END LINE  Q:QUIT
A:ADD    R:REMOVE
```

In the middle of the screen you see a cursor, consisting of four flashing dots. Near the bottom you see a horizontal line with a ground symbol attached. This is your ground line.. Eventually your circuit must connect to it. Below the ground line is the COMMAND MENU.

The complete definition of each command is as follows:

COMMAND	NAME	FUNCTION
I	UP	Moves cursor up one grid in normal mode, up 1/4 grid in the Line mode.
M	DOWN	Moves cursor down one grid in normal mode, down 1/4 grid in the Line mode.
J	LEFT	Moves cursor left one grid in normal mode, left 1/4 grid in the Line mode.
K	RIGHT	Moves cursor right one grid in normal mode, right 1/4 grid in the Line mode.
A	ADD A COMPONENT	Initiates component adding routine. Requires user to specify component type, direction and parameter value. Draws the selected component and adds it to the circuit description.
R	REMOVE A COMPONENT	Initiates component removal routine. Requires user to specify component type and direction. Erases the selected component and eliminates it from the circuit description.

COMMAND MENU

COMMAND	NAME	FUNCTION
S	SHORT	Requires the user to specify the direction of the short and then draws a shorting bar between the node the cursor was initially on and the node immediately adjacent and in the direction specified. Positions the cursor at the output node (other end of the short).
B	BEGIN LINE	Puts the system in the Line mode. A line is an extended short between two nodes. While in the Line mode the system recognizes only the I, J, K and M cursor commands and the E: END command. This command is used to short together two widely separated nodes. The short will connect the node the cursor was initially on and the node at the cursor position when the E command is given. During the Line mode the cursor plots a trail and moves in 1/4 grid increments allowing the user to draw the shorting line between intervening components and around intervening nodes, allowing greater drawing clarity.
E	END LINE	Terminates the line mode. Creates a short between the initial node and the node the cursor is currently at. Positions the cursor at the terminal end of the line short. Cursor must be on a node (not between) to terminate a short.
Q	QUIT	Terminates the drawing process. Allows user the option of saving the circuit on the drawing board. Returns control to the DESIGNER main menu.

COMPONENT TYPES

Components to be added or deleted are specified by typing the 1st 3 letters of their proper name. The complete list and their respective symbols are as follows:

BATTERY

BAT

RESISTOR

RES

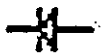
CAPACITOR

CAP

INDUCTOR

IND

DIODE



DIO

SINUSOIDAL SOURCE

VSI

PROGRAMMABLE SOURCE

V(T)

Uxe a meno.

NPN TRANSISTOR

NPN

PNP TRANSISTOR

PNP

LINE SHORT

N/A

Non è possibile cancellare.

NMOS TRANSISTOR

NMO

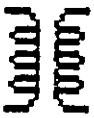
PMOS TRANSISTOR

PMO

OP AMP

OPA

TRANSFORMER



TRA

SHORT

SHO OR S

SWITCH

SWI

USER SOURCE

USE

Programma esterno

POLYNOMIAL SOURCE

POL

10 TO - 1000 basic

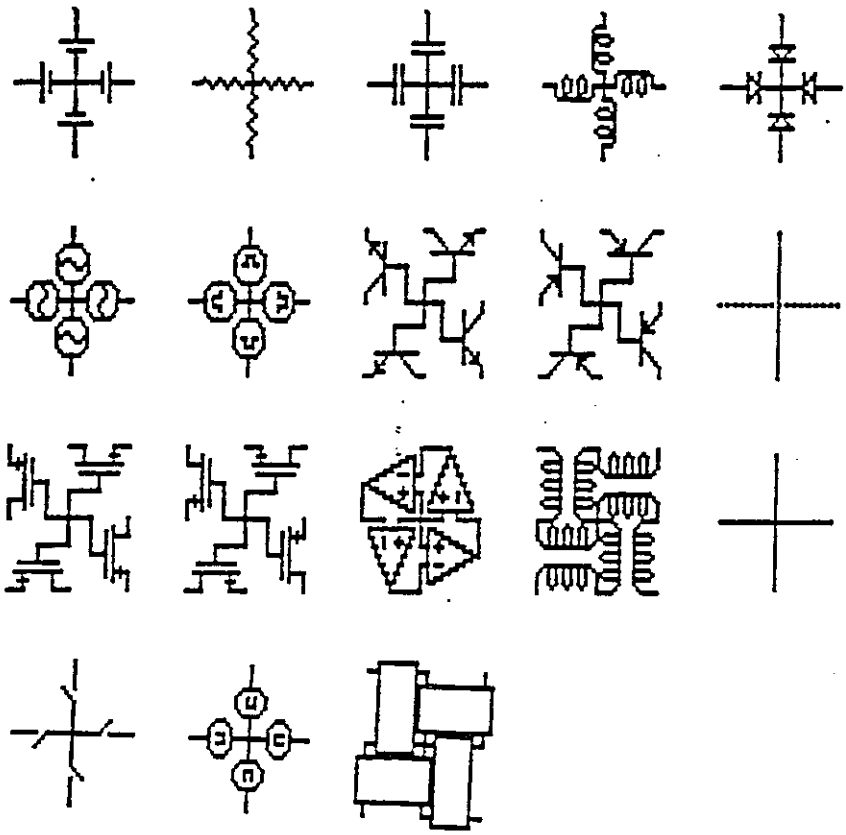
ORIENTATION DEFINITION

In order to add or remove a component you must specify the direction of the component. The direction of a component is determined by an imaginary vector pointing from the input side to the output side. For two-terminal components the vector direction is from the negative side to the positive side.

For 3 and 4 terminal components the vector points from the positive input lead (eg. base, gate lead) to the positive output lead (eg. NPN collector PNP emitter, NMOS drain, PMOS Source, etc.).

As you specify R,D,L & U, the vector rotates clockwise creating an angle (relative to the horizontal) of 0, -90, -180, -270 respectively.

The following is a compilation of each of the components drawn in each of the 4 possible directions from the same center starting point.



ADDING AND REMOVING SHORTS

Please note that there are three different ways of creating a short between two nodes.

1: By using the Add (A) command and using "SHO" as the component.

2: By using the Short (S) command. This is generally quicker and does not require specifying a parameter.

3: By using the Begin Line and End Line commands. Simply position the cursor on the first node, press B, move the cursor (plotting a line as you go) to the second node and press E.

While there are three ways to short nodes together, there is only one way to delete a short - by using the Remove Command (R). To delete a short, you position the cursor on the same node it originated on, press R, enter "SHO" for the component name, specify the direction from the first node to the second and press return. Note that this command will remove only normal shorts. Shorts generated by the Begin/End routine cannot be eliminated, so use them with care.

CLEARING THE SCREEN-APPLE

If you wish to clear the screen and start again, press Q for Quit, select 4 on the Epilog menu and control passes to the Main Menu, clearing the circuit description in the process. Select option 1 to start a new circuit diagram.

CLEARING THE SCREEN-IBM

If you wish to clear the screen and start again, press Q for Quit, respond with N to file query and select option 1 from the Designer Main Menu to start a new circuit diagram.

RETRIEVING OLD CIRCUIT FILES

In using the DESIGNER you will usually want to work on the drawing during several sessions. Each time you quit you're given the option of filing the circuit diagram. If you elect to do so, you're asked for the name to file the drawing under. The program files your drawing and its' circuit description in a disk file using the name you gave it. When you return to the DESIGNER module you can pick up where you left off by using option 2 from the DESIGNER main menu. Simply enter the name you used to save the circuit under and the program retrieves the circuit description and it's associated picture (drawing) allowing you to continue where you left off.

GENERAL GUIDELINES

1. Periodically delete your old circuits. Each drawing uses up 8 to 10K bytes of diskette storage space on the Apple and 16 to 18K bytes on the IBM. There is sufficient room on the diskette to store 7 to 12 files. To delete files simply use option 3 from the DESIGNER main menu and enter the name of the file to be deleted.

2. Don't short out components. Remove them instead.

3. Don't leave components hanging (eg. one or more nodes not connected to anything).

4. Use the lowest nodes on the screen where possible. This will reduce the compacting time. Compacting is the process of removing unused nodes and interpreting shorts.

5. Don't use more than the maximum number of components or the maximum number of nodes. The maximums are specified in the Appendices. Shorts and nodes used as intermediates in shorts are excluded from the node and component counts.

6. When deleting a component, position the cursor on the same grid as it occupied when you originally created it.

COMMAND PRACTICE

To illustrate the use of the commands let's start a new circuit diagram. From the DESIGNER main menu select option 1. First use the I, J, K and M keys to move the cursor around. When you feel comfortable with these keys use them to move the cursor to the ground line at just the point where the ground symbol is attached.

Now press the "A" key, type in BAT (Battery), direction U (Up), and enter a parameter value of 10. You have just entered a 10 volt battery. Let's suppose that you really wanted a 9 volt battery. Press R (Remove), BAT (Battery) and D (Down). The system will beep and print the message:

NO DEVICE TO DELETE. RE-SPECIFY!

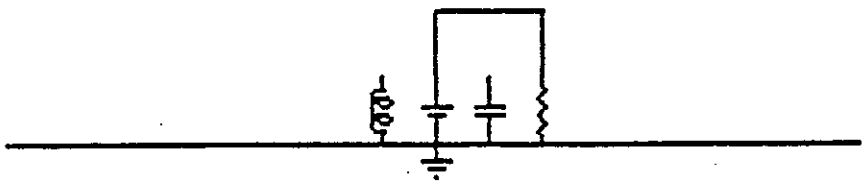
It does this because you must always remove components from the point at which they were originally added. To remove this battery move the cursor down one grid by pressing "M". Now enter "R", BAT, and "U". Presto, the BATTERY is gone! Now add it back by using the sequence: A, BAT, U, 9.0. Presto, it's back where it was, this time having a value of 9 volts.

Note that each time you add a new component, the system positions the cursor at the "output" point of the component, anticipating your desire to continue drawing from that point. Note also that components are always added or deleted from the current cursor position. Think of the cursor as the tip of your drawing pen.

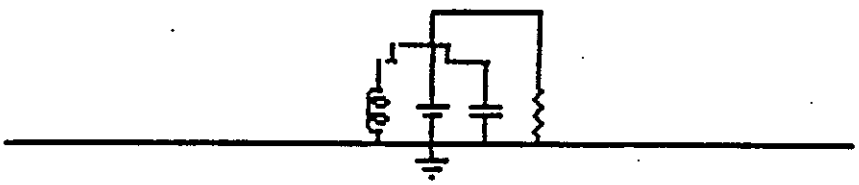
Now let's illustrate the Short. The Short is treated like any other component. It can be added or deleted. To illustrate enter the following sequence: A, SHO, U, and the system will draw a vertical line. Note that no parameter was required.

Now enter the sequence: A, SHO, R and the system will draw a line to the right. Actually there is an easier way to draw simple shorts. Press "S" then "R" and the system will draw another shorting line to the right. Try it again with "S" and "D". Now add a resistor to ground with the sequence: A, RES, D, 10.

Now move the cursor to the left with "J" and up with an "I". Add a capacitor to ground with the sequence: A, CAP, D, 1E-10. Move the cursor two grids to the left with "J", and "J". Next add an inductor with the sequence: A, IND, U, 1E-6. Your picture should now look like this:



Suppose you wanted to connect the inductor to the top plate of the capacitor. You can't use the SHORT because that will connect the inductor to the top plate of the battery. Instead you use the BEGIN LINE/END LINE commands. To illustrate, press "B". Now press "I". Note that the cursor moves up only 1/4 grid and plots a short line. Now press "K", "I", "K", "K", "K", "K", "M", "K", "K", "K", "M". At this point the cursor should be positioned at the top of the capacitor. Now press "E" to end the SHORT. You have just shorted the inductor and capacitor together using the BEGIN/END COMMANDS. Your picture should now look like this:



Note that the extra jags we used were not necessary. The important point is that in the BEGIN/END LINE mode the cursor moved in 1/4 grid increments, allowing you to draw around the major grid points where other components might be connected (eg. The battery in this case).

EPILOG OPTIONS-APPLE

If your system is an APPLE there are a variety of options available when you press Q from the command menu. These are summarized in the Epilog menu.

1. SAVE PICTURE TO DATA DISK.
2. SILENTYPE DUMP.
3. MX-80 DUMP.
4. GRAPHICS CARD DUMP.
5. NONE OF THE ABOVE.

Select option 1 and the system will respond with:

```
HIT RETURN TO SAVE THIS CIRCUIT UNDER
THE FILE NAME XXXXX

OR ENTER A NEW FILE NAME
?.....
```

Pressing (RETURN) causes the system to file the circuit diagram for later retrieval under the last used circuit name XXXX. Type in any other name to file it under a new name. Names should not exceed 30 characters and should begin with a letter of the alphabet (no numbers).

Selecting option 2 or 3 from the Epilog menu will cause the system to create a graphics dump on your Silentype or MX-80 printer (if equipped with Graphtrax).

Selecting option 4 will cause the system to request:

"ENTER THE DECIMAL CODES TO ACTIVATE GRAPHICS PRINTER"

```
N1=
N2=
N3=
N4=
```

The user then enters the decimal codes that activate the graphics card options for his particular card type.

The system will then issue two print statements.

1. PRINT CHR$(4); "PR#"; STR$ (PRINTER SLOT)
2. PRINT CHR$(N1); CHR$(N2); CHR$(N3); CHR$(N4)

If N3 or N4 are zero the corresponding CHR$( ) portions are omitted.

For example if you have the GRAPPLER + card you would enter:

```
N1=9     (eg. CTRL I)
N2=71    (eg. "G")
```

If you wanted a double size version you would add:

```
N3=68    (eg. "D")
```

For more information consult your graphics card instruction manual as the particular choice of N1, N2, N3, and N4 will vary with each card.

EPILOG OPTIONS-IBM

For the IBM pressing Q from the Command menu automatically invokes the message:

```
HIT RETURN TO SAVE THIS CIRCUIT UNDER
THE FILE NAME XXXXX

OR ENTER A NEW FILE NAME
?.....................
```

Pressing (RETURN) causes the system to file the circuit diagram for later retrieval under the last used circuit name XXXX. Type in any other name to file it under a new name.

Names should be 8 characters maximum and should contain no spaces or leading numeric characters. There is no specific graphics dump program command. However, if your system has the latest version of DOS 1.1 or 2.0 then the SHIFT/PRT SC will automatically dump the HI-RES drawing to your IBM dot matrix or EPSON MX-80 printer if you have executed the DOS extension program called "GRAPHICS" located on your DOS System master diskette, prior to running MICRO-CAP. Of course you must press the SHIFT/PRT SC keys before exiting the Command menu or else the picture will be gone.

ERROR MESSAGES

1. BEGIN/END: Attempting to use the "E" (END) command while the cursor is not on a major grid will cause the error message:

   LINE END MUST BE ON A GRID POINT.

2. Attempting to read or delete a non-existant file will produce the error message:

   NO SUCH FILE EXISTS.

3. Attempting to save a picture file to a data disk that is full produces the message:

   DISK FULL, INSERT NEW DATA DISK
   AND PRESS RETURN.

III THE ANALYZER MODULE

Option 2 on the MAIN DISK MENU is used to load and run the ANALYZER module. This module does all of the real number crunching. It's main menu gives these options:

ANALYZER MENU

MICROCOMPUTER CIRCUIT ANALYSIS PROGRAM

1:SAVE/RETRIEVE/DELETE NETWORK FILE

2:CREATE/REVIEW/EDIT NETWORK

3:TIME DOMAIN (TRANSIENT ANALYSIS

4:FREQUENCY DOMAIN (AC) ANALYSIS

5:TRANSFER (DC) ANALYSIS

6:REVIEW/EDIT STANDARD COMPONENTS

7:GENERATE USER DEFINED SOURCES

8:SETUP PRINTER

9:RETURN TO MAIN MENU

In this section we will review Options 1, 2, 6, 7, and 8. Options 3, 4, and 5 will be reviewed in subsequent chapters.

1:SAVING/RETRIEVING/DELETING NETWORK FILES

This option is used to retrieve Network files from the data diskette. These files may have been generated by the DESIGNER module or by the ANALYZER module. As we shall see the ANALYZER module has an editor that can create and modify circuit files.

To use option 1 press "1" and the system will respond with the question:

```
SAVE (S), RETRIEVE (R), OR DELETE (D)
A NETWORK FILE?
```

To illustrate press "R" and the system will respond with:

```
PRESS (RETURN) TO SELECT THE FILE NAME XXXXXXX

OR ENTER A NEW NAME?
```

Type in BRC (RETURN) and the system will read the BRC file and return control to the Main Menu. If you wished to save a circuit file and had just created or modified it (using Option 2) you would have used the same sequence except you would have used "S" instead of "R". Similarly to delete a file you use the "D" instead of "S" or "R". Note that there are two distinct kinds of files for each network.

1. DESIGNER File
2. ANALYZER File

When you delete a file using the ANALYZER it does not delete the DESIGNER version of the same file name. When you delete a file using the DESIGNER both types of files are deleted from the data diskette.

2:CREATING/REVIEWING/EDITING NETWORKS

Although the DESIGNER module is normally used to generate circuits, the Network Editor can also be used. It can create new circuits or edit old ones simply by creating the Netlist. Circuits created in this fashion will, of course, not have a circuit diagram. The Network Editor, creates a display of the Netlist of the circuit file. A Netlist is simply a list of each component in your network, its' interconnection to the nodes in the network and its' parameter or type. The Netlist is displayed as a form that looks like this:

NETLIST

REGULATED POWER SUPPLY CIRCUIT

REF	COMPONENT	CONNECTIONS				PARAMETER
		IN		OUT		OR
NO.	NAME	-	+	-	+	TYPE
1:	TRANSFORMER	0	1	3	7	0
2:	DIODE	7	0	0	0	0
3:	DIODE	6	7	0	0	0
4:	DIODE	6	3	0	0	0
5:	DIODE	3	0	0	0	0
6:	RESISTOR	6	4	0	0	1000
7:	DIODE	4	0	0	0	3
8:	OPAMP	2	4	0	5	0
9:	NPN TRANS.	0	5	2	6	0
10:	RESISTOR	2	0	0	0	100
11:	CAPACITOR	2	0	0	0	1E-4
12:	VSIN	0	1	0	0	0

UP DOWN ADD EDIT REMOVE PRINTER QUIT

At the top are displayed the circuit name and the names of the 7 data fields used to describe each component. The definition of each field is as follows:

FIELD	DEFINITION
REF NO.	An index number used to identify the component for each line.
COMPONENT NAME	A label used to identify the type of component for each line. Following are the only legitimate names (components):

NMEMONIC	COMPONENTS
BAT	BATTERY
RES	RESISTOR
IND	INDUCTOR
CAP	CAPACITOR
DIO	DIODE
NPN	NPN TRANSISTOR
PNP	PNP TRANSISTOR
NMO	NMOS TRANSISTOR
PMO	PMOS TRANSISTOR
VSI	SINUSOIDAL VOLTAGE SOURCE
OPA	OP AMPS
V(T)	PROGRAMMABLE VOLTAGE
TRA	TRANSFORMER
SWI	SWITCH
USE	USER SOURCE
POL	POLYNOMIAL SOURCE

When using this field it is only necessary to type in the first 3 characters of the name for it to be properly recognized.

CONNECTIONS IN-: The node number of the most negative side of the component. For two terminal elements, R,L,C, the choice is arbitrary for positive or negative lead. For OPAMPS this is the bottom input lead (OPAMP - terminal). For transformers this is the bottom lead of the primary coil.

CONNECTIONS IN+: The node number of the positive side of the component. For Bipolar transistors this is the base lead node number. For MOS devices this is the gate lead node number. For OPAMPS this is the top input terminal (OPAMP + terminal).

CONNECTIONS OUT-: For NPN transistors this is the emitter lead node number. For PNP transistors this is the collector lead node number. For NMOS devices this is the source lead node number. For PMOS devices this is the drain lead node number. For transformers this is the bottom lead of the secondary coil.

CONNECTIONS OUT+: For NPN transistors this is the collector lead node number. For PNP transistors this is the emitter lead node number. For NMOS devices this is the drain lead node number. For PMOS devices this is the source lead node number. For transformers this is the top lead of the secondary coil. For OPAMPS this is the output lead.

PARAMETER OR TYPE: For Standard Components this is the type number. For example if the current line was to be an NPN transistor, Type 3, you would enter 3 here.

PARAMETER OR TYPE (CONT): For resistors this is the value of the resistance (in OHMS). For capacitors this is the value of the capacitance (in Farads). For inductors this is the value of the inductance (in Henrys). For batteries this is the value of the D.C. voltage (in Volts). You must use scientific notation to enter these values. For example a capacitor of 1 micro-farad would be entered as 1E-6. An inductor of 4mh would be entered as 4E-3. A voltage of 7.8 volts would be entered as 7.8. For Switches this field is used to specify the turn-on & turn-off conditions (see Component Models).

2:CREATING/REVIEWING/EDITING NETWORKS

ADD COMMAND

To add a component you simply press the key "A". Select it and the cursor immediately positions itself at the next available input line. It then prints the reference number of the component value you're about to enter. For now let's create a circuit description of the BRC circuit discussed earlier. Press "A" and BAT (RETURN). The program will display the full name of the component (battery) and then move the cursor to the next field. Enter 0 for the negative IN connection and 1 for the positive IN connection. Notice that the cursor skips over the next two fields, as they are not required to define a battery. In general the cursor will lead you to just the fields you need to enter. The next field the cursor stops at is the Parameter or Type field. Enter 10 (for 10 volts) and you've just completed your first component entry.

Before we go any further you may be wondering where we get the node numbers. Refer back to the original drawing and you'll see that we've labeled the three nodes 0, 1, and 2. Zero is always used for the ground node (most negative node of the circuit). In general when using the Editor to enter circuits, draw your circuit diagram, label the nodes sequentially from zero on up (don't skip any node numbers) and label the components from 1 on up. To clarify your diagram, circle the node numbers but not the component numbers. Then with a completed diagram simply key in the description.

To continue, let's finish the BRC circuit description. Select "A" and type in RES (RETURN). The resistor is connected between Nodes 2 and 1 so enter them and when the cursor is at the Parameter field, enter 100 (or 1E 2) for 100 OHMS. Next enter the capacitor with a value of 1E-10 (100 Pf) connected between Nodes 0 and 2.

REMOVE COMMAND

Now, let's use the REMOVE command. Select R:REMOVE. The program will then ask you which item is to be deleted. Select 1 (the battery) and then (RETURN). The program will then reprint the entire page after deleting the first component. If you select 0 for the component to be removed, the program deletes all entries and clears the screen.

EDIT COMMAND

Now let's use the EDIT Command. Select E:EDIT. The program requests the branch number to be changed (reference # on the left). Select the resistor (2) for editing and hit (RETURN). The cursor will now start at the first data field and await your response. To edit any particular field simply press "E" (no RETURN) and type in the new value (or name). Pressing any other key will SKIP that field and move to the next field and await your decision to EDIT or SKIP. Note that the cursor moves to all fields - even those which have no data in them (and aren't even used for this componet). To illustrate the editing, press (RETURN) until your cursor is at the parameter field and then press "E". Then type in a new value for the resistor - for example 1000 (for 1000 OHMS). When you're finished with the last field, control passes to the COMMAND MENU at the bottom.

2:CREATING/REVIEWING/EDITING NETWORKS

NETWORK EDITOR: UP AND DOWN COMMANDS

If your circuit description requires more than 16 lines you will have to use the UP and DOWN commands. The D:DOWN command simply displays the next highest page of 16 lines in the Netlist. The U:UP command displays the next lowest page of 16 lines. The system will allow a maximum of 6 pages or 96 lines to describe your circuit.

NETWORK EDITOR: PRINTER COMMANDS

If you have a printer, pressing "P" will cause the system to create a printed copy of the NETLIST. Make sure that your printer slot is correctly set (option 7 ANALYZER main menu).

NETWORK EDITOR: QUIT COMMAND

Pressing "Q" passes control to the ANALYZER main menu.

6:STANDARD COMPONENT EDITOR

Option 6 on the ANALYZER main menu is used to review or edit your Standard Component model parameters. When Networks are built using Standard Components the type number (0-4) is used to specify which of the 5 types of the Standard Component is to be used. This editor allows you to modify the parameters of each type. When you select option 6 the system will display the following menu:

STANDARD COMPONENTS

0. OPAMPS

1. DIODES

2. BIPOLAR TRANSISTORS

3. MOS TRANSISTORS

4. PROGRAMMABLE WAVEFORMS

5. SINUSOIDAL SOURCES

6. TRANSFORMERS

7. POLYNOMIAL SOURCES

8. PRINTER COPY OF STANDARDS

9. RETURN TO MAIN MENU

YOUR CHOICE?

6:STANDARD COMPONENTS EDITOR

There are 8 Standard Components. Select 1: Diodes, and the program will display the parameters of the first diode type (type 0). Press "R" and the display increments to Type 1.

```
                DIODES
                TYPE 1

0:  Saturation Current (IO)      2E-09
1:  Zener Voltage                  130
2:  Zener Resistance                10
3:  Series Resistance                3
4:  Parallel Resistance           1000
5:                                   0
6:                                   0
7:                                   0
8:                                   0
E:EDIT  R:REVIEW NEXT TYPE   Q:QUIT
```

This display shows the parameter # on the far left, the name of the parameter in the middle and the value of the parameter for the diode type currently displayed. Thus the Zener voltage of diode Type 1 is 130 volts and so on. The parameters in this case are self-evident but in general you should familiarize yourself with the models used to approximate the Standard Components and how these parameters relate to the models. You can do so by reviewing the Components Models section of this manual where the models are described.

At the bottom of the display you will see a menu of choices. If you wish to edit any particular parameter on this page, press "E". The system will respond:

SYSTEM	TYPICAL USER RESPONSE
Enter the # of the item to be edited.	Enter the parameter # to be modified (e.g., 1 for Zener Voltage).
Enter the new value.	Enter 25 (for 25 volts).

Following your entry, the system re-displays the page showing your edited value. Later when you return to the Main Menu the system will re-file the standards in a diskette data file if any edits have been made.

R:REVIEW on this page's menu allows you to review the next diode type. Press "R" and the system displays the parameters of the next diode type (type 2). Continuously depressing the "R" key cycles the display through diodes Types 0-4 and then back to Type 0.

Q:QUIT returns you to the Standard Components menu where you may review other types of Standard Components or by using option 9 return to the Main Menu. For now select Q:QUIT to return and select "2" to review the parameters of the first bipolar transistor. They should look something like this:

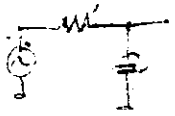
```
BIPOLAR TRANSISTORS
      TYPE 0

0:BETA (HFE)                        50
1:BASE EMITTER DIODE TYPE #         1
2:F-TAU=U NITY GAIN BANDWIDTH       1E8
3:COLLECTOR CURRENT (HFE,FT)        1E-03
4:SATURATION RESISTANCE             5
5:CAPACITANCE B-E                   3.06E-11
6:CAPACITANCE C-B                   3.E-11
```

Beta, of course, is the current gain of the bipolar transistor. Parameter #2 is the standard diode type to be used in modeling the transistor. Parameter 3, F-TAU, is the unity gain bandwidth. Parameter 4 is the collector current at which BETA and F-TAU have been measured. It is not necessarily the maximum current expected. Parameter 4 is the Saturation Resistance of the output port, the ratio of VCE to ICE when the transistor is in saturation. Parameter 5 is the base-emitter capacitance. It is calculated by the program from the parameters IC and F-TAU.

If you have a printer connected review the remaining components by selecting option 8 on the STANDARD COMPONENTS EDITOR MENU. Selecting this option will cause the Standard Components Library to be printed on your printer. Before you use this command set the printer slot (APPLE only) using option 7 on on the ANALYZER MAIN MENU.

SAMPLE STANDARD COMPONENTS LIBRARY



STANDARD COMPONENTS

OPAMPS

PARAMETER NAME	TYPE 0	TYPE 1	TYPE 2	TYPE 3	TYPE 4
INPUT RESISTANCE	1000000	1000000	1000000	10000	100000
OPEN LOOP GAIN	1000	1000	2000	2000	10000
OUTPUT RESISTANCE	100	100	1000	1000	200
INPUT OFFSET VOLTAGE	1E-04	1E-04	1E-04	2E-03	1E-03
MAXIMUM OUTPUT VOLTAGE	30	10	30	30	30
OUTPUT CAPACITANCE	5E-08	5E-09	1E-08	1E-08	1E-08

DIODES

PARAMETER NAME	TYPE 0	TYPE 1	TYPE 2	TYPE 3	TYPE 4
SATURATION CURRENT(IO)	1E-15	1E-12	1E-12	1E-13	1E-12
ZENER VOLTAGE	130	200	60	5	5
ZENER RESISTANCE	10	20	10	10	10
SERIES RESISTANCE	1	1	1000	10	10
VT TERM (VT=K*T/Q)	.026	.026	.025	.026	.025
PARALLEL RESISTANCE	1000000	10000	1000000	10000	10000

BIPOLAR TRANSISTORS

PARAMETER NAME	TYPE 0	TYPE 1	TYPE 2	TYPE 3	TYPE 4
BETA (HFE)	66	50	50	40	50
BASE EMITTER DIODE TYPE #	0	1	2	2	1
F-TAU=UNITY GAIN BANDWIDTH	125000000	200000000	50000000	80000000	500000000
COLLECTOR CURRENT (HFE-FT)	2E-03	2E-03	1E-03	.01	2E-03
SATURATION RESISTANCE	5	3	5	10	5
CAPACITANCE B-E	9.794E-11	6.12100001E-11	3.672E-10	7.651E-10	2.448E-11
CAPACITANCE C-B	1E-12	1E-12	1E-11	1E-10	1E-11

MOS TRANSISTORS

PARAMETER NAME	TYPE 0	TYPE 1	TYPE 2	TYPE 3	TYPE 4
BETA FACTOR (K'*W/L)	.01	.01	1E-03	1E-03	1E-05
THRESHOLD VOLTAGE	2	-2	-2	2	2
GATE-DRAIN CAPACITANCE	1E-11	1E-11	1E-11	1E-11	5E-13
GATE-SOURCE CAPACITANCE	1E-11	1E-11	1E-11	1E-11	1E-12
DRAIN-SOURCE RESISTANCE	1000000	1000000	100000	100000	1000000
DRAIN-SOURCE CAPACITANCE	1E-11	1E-12	1E-11	1E-11	1E-12
LINEAR TRANSCONDUCTANCE(GM)	.05	.05	5E-03	5E-03	5E-05

PROGRAMMABLE WAVEFORMS

PARAMETER NAME	TYPE 0	TYPE 1	TYPE 2	TYPE 3	TYPE 4
ZERO LEVEL VOLTAGE	0	0	.5	.5	0
ONE LEVEL VOLTAGE	5	5	5	5	5
TIME DELAY TO LEADING EDGE	1E-08	1E-08	2E-06	1E-07	1E-04
TIME DELAY TO ONE LEVEL	1E-05	2.55E-07	3E-06	1.1E-07	2E-04
TIME DELAY TO FALLING EDGE	1.2E-05	5E-07	7E-06	5E-07	5E-04
TIME DELAY TO ZERO LEVEL	1.3E-05	5.5E-07	8E-06	5.1E-07	6E-04
PERIOD OF WAVEFORM (1/F)	2E-04	1E-06	1E-05	1E-06	1E-03

SINUSOIDAL SOURCES

PARAMETER NAME	TYPE 0	TYPE 1	TYPE 2	TYPE 3	TYPE 4
SINE FREQUENCY	60	500000	2000000	100	0
AMPLITUDE/2	60	.5	.05	10	616
D.C. VOLTAGE LEVEL	0	0	0	10	0
PHASE ANGLE(RADIANS)	0	3.14159	0	1.5	0
SOURCE RESISTANCE	1	1	1	.1	.1
PERIOD	0	0	0	0	0
TIME CONSTANT	0	0	0	0	0

TRANSFORMERS

PARAMETER NAME	TYPE 0	TYPE 1	TYPE 2	TYPE 3	TYPE 4
INPUT SELF-INDUCTANCE	.01	5E-08	5E-04	10	10
CURRENT GAIN (TURNS RATIO)	6	10	10	10	10
COEFFICIENT OF COUPLING	.99	.98	.98	.98	.98
RES-SECONDARY	1E-03	.1	.1	.1	.1

POLYNOMIAL SOURCES

PARAMETER NAME	TYPE 0	TYPE 1	TYPE 2	TYPE 3	TYPE 4
A	0	0	0	0	0
B	-1E-03	5E-04	1E-03	.01	2E-04
C	1	1	1	1	1
D	0	0	0	0	0
E	0	0	0	0	0
F	0	0	0	0	0
G	0	0	0	0	0

8:GENERATING USER DEFINED SOURCES

This option allows the user to create his own unique voltage waveforms for use as driving sources in a Transient Analysis. To use it the user must be familiar with the BASIC language as he is required to modify a BASIC program in order to generate his unique waveform file.

The program, called WAVEGEN, contains all of the necessary program code to create, display and file a user waveform. The user supplies only the BASIC code that actually calculates the waveform voltage as a function of time.

A section in the program (lines 1000-2000) is reserved for the user code. All that is necessary is for the user to place in the user area a BASIC line (or lines) containing a formula for calculating the voltage waveform. For example the program is supplied with a typical user line 1500 that generates an exponentially decaying sinusoidal voltage waveform. In particular line 1500 reads:

```
1500 V= 5*EXP(-T/2E-7)* SIN(T/2E-8)
```

The variable V stands for the voltage of the waveform and T represents time. The implied units are volts and seconds.

When you run WAVEGEN you have this initial option:

"PRESS M TO MODIFY THE WAVEFORM CODE OR ANY OTHER KEY TO GENERATE THE DISK FILE".

8:GENERATING USER DEFINED SOURCES

If you press M the system will print the message:

THE USER AREA BEGINS AT LINE 1000 AND ENDS AT 2000. YOU MAY PLACE ANY BASIC CODE IN THE USER AREA, INCLUDING FUNCTIONS, DATA STATEMENTS, EQUATIONS ETC. THE USER CODE GENERATES THE WAVEFORM.

AS SUPPLIED THE USER CODE CONTAINS A DEMO FUNCTION WHICH GENERATES AN EXPONENTIALLY DECAYING SINUSOID, USING LINE 1500.

REMOVE LINE 1500 BEFORE INSTALLING YOUR CODE.

AFTER PLACING YOUR CODE IN THE USER AREA, TYPE RUN, PRESS <ENTER> TWICE AND THE PROGRAM WILL ENTER THE GENERATE MODE.

REMEMBER, UNLESS YOU SAVE THE BASIC PROGRAM UNDER THE NAME..WAVEGEN AFTER MODIFYING THE USER CODE AND BEFORE ACTUALLY GENERATING THE WAVEFORM, YOUR USER CODE WILL BE LOST.

A typical usage begins with pressing M. The user then modifys the user area to generate a new waveform, types "RUN" (RETURN), press (RETURN) again and the waveform generation process begins.

First the system asks:

ENTER TMAX FOR THE WAVEFORM.

The user types in the time duration of the waveform. For the demo code a suitable choice would be 1E-6 (one micro-second).

The system then asks the user to:

ENTER THE FILE # TO SAVE WAVEFORM UNDER (0-9).

The user enters the desired file # and presses (RETURN).

Finally the system requests the maximum peak to peak amplitude of the waveform. This last request is needed so that the waveform may be suitably scaled for plotting during the creation of the user source disk file. It has no effect on the contents of the actual user file.

Following the last entry the system calculates the waveform, plots it on the screen and saves it on the data diskette.

The system actually calculates the specific values by setting T=0, incrementing T by DT, where:

DT= TMAX/1000,

calling the user subroutine code to calculate the value of V for the current value of T, and filing the waveform in 10 files by the name:

```
USER F0
USER F1
USER F2
USER F3
USER F4
USER F5
USER F6          F= File Number selected
USER F7
USER F8
USER F9
```

where each file contains 100 sequential voltage values. The Transient Analysis routine can access these files if a particular network requires a user source. It can also capture a waveform generated during a simulation and dump it into another user file.

Following completion of the waveform generation the user is automatically returned to the Analyzer Main Menu in the Apple version. In the IBM version the user must type:

```
SYSTEM <RETURN>
EDITOR <RETURN>
```

and control will then pass to the Analyzer Main Menu.

CREATING NEW DATA DISKS

MICRO-CAP is supplied with a data disk which contains sample circuits. The diskette is nearly full and one of the first things you will want to do is to create a new data diskette.

To do so you must begin with a blank disk. First initialize the diskette. For APPLE this means you must perform an INIT command. If you are unfamiliar with the procedure read pages I3 and I4 of the APPLE II DOS MANUAL.

If your system is an IBM you must run the FORMAT program. The procedure for doing this is explained on pages 3-38 to 3-40 of the DISK OPERATING SYSTEM MANUAL. Use the plain FORMAT option (eg. no S parameter).

Both of these procedures clear the disk and format it for their respective DOS. Once the initialization is complete one more step remains.

A data diskette must contain a copy of the MICRO-CAP STANDARDS FILE. To get one on the disk you must follow this procedure.

1. Using the supplied program and data diskette, go to the ANALYZER main menu. From here select option 6: STANDARD COMPONENTS.

2. Select any of the components by pressing 0 to 6.

3. Press the "E" (for EDIT) key.

4. Edit any of the component values (usually you will want to replace it with the same value).

5. Press "Q". You should now be at the STANDARD COMPONENTS menu.

6. Replace the original data diskette with your new (blank) data diskette.

7. Press "9" (RETURN TO MAIN MENU).

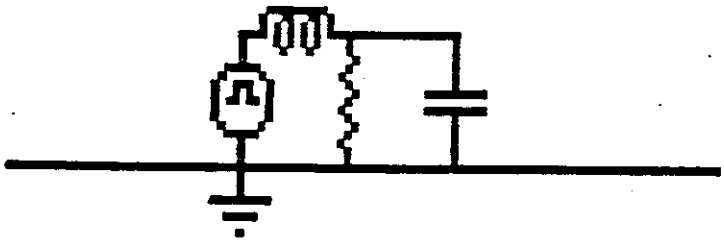
Following this last step the system will write the entire STANDARDS file on the data diskette which of course is the new one. At this point your new diskette is ready to store new circuit files. This same procedure may be used to transfer Standards Files between data diskettes. Selecting option 6 from the ANALYZER main menu forces the system to read the Standards File currently in the secondary drive. Subsequent editing and returning to the ANALYZER menu forces the system to write out the entire Standards File to whatever disk happens to be in the secondary drive.

IV TRANSIENT ANALYSIS

PROLOGUE

To perform a TRANSIENT ANALYSIS you must begin at the ANALYZER main menu. First you must have a circuit file in memory. To get a circuit file in memory you must either retrieve one from the data disk (option 1 of ANALYZER menu), or create one using the Network Editor (option 2 of ANALYZER menu).

If you haven't already done so, retrieve from your data disk the file PRLC. Its' circuit is:



Check to make sure it's in memory by using option 2 to display it. Then return to the ANALYZER main menu with "Q" amd select option 3: TRANSIENT ANALYSIS.

As soon as you press 3 the system runs the TRANSIENT ANALYSIS prologue routine. A flow chart of the prologue looks like this:

ENTER ANALYSIS
LIMITS

OPTIONAL RESET OF
INITIAL CONDITIONS

OPTIONAL PRE-SET OF
INITIAL CONDITIONS

WAVEFORM DUMP OPTION

SELECT DISPLAY
MODE

The simulation parameters are entered on a display form that looks like this:

PROLOGUE

ANALYSIS LIMITS

PRESS (RETURN) TO ACCEPT DEFAULT VALUES OR TYPE DESIRED VALUE AND PRESS (RETURN).

MAXIMUM SIM TIME (SEC)	1E-06
MAXIMUM DELTA TIME (SEC)	1E-08
MINIMUM ACCURACY (%)	5
UPPER TRACE NODE(S)	1
OFFSET FOR #1	0
SCALE FACTOR FOR #1	1
LOWER TRACE NODE(S)	2
OFFSET FOR #2	0
SCALE FACTOR FOR #2	1

The first item is the maximum simulation time. When a simulation (or Transient Analysis) is run it starts at T (TIME) = 0 and runs to T = TMAX. What the system wants to know here is the value of TMAX.

The second item is the time increment or Delta Time to be used in the simulation. Actually it is the maximum value. Specifying a very small DELTA T (relative to your circuit time constants) will produce a very long simulation time (in real time) and generally a more accurate result. Specifying a large DELTA T will have the opposite effect. In general keep DELTA T less than the smallest time constant in your system. For example a suitable choice for our PRLC circuit would be 5 to 10ns.

The third item in the prologue is the MINIMUM ACCURACY. As the simulation proceeds the program automatically adjusts DELTA T up and down. If the voltage change exceeds:

$$\frac{ACC}{100} \times \text{SCALE FACTOR} \times 10$$

then the system will lower DELTA T to produce a smaller voltage change for the next printout. Conversely it will increase DELTA T if things are moving to slow. The variable ACC tells the program when too much or too little voltage change has occurred. In general 1 to 5% are appropriate choices here.

When you run a TRANSIENT ANALYSIS it is possible to monitor on the video display (or the printer plot) two of the nodes in the circuit. Prologue items 4, 5, & 6 specify:

a) Which node to monitor on the upper trace.

b) How much voltage to add or subtract to the actual voltage calculated before displaying the result.

c) What scale factor to use in volts per division (there are 10 divisions full scale).

Similarly items 7, 8, & 9 are the same type of information but for the 2nd displayed node.

To make your selection you may either accept the default values (which are saved from the last analysis run) by pressing (RETURN) or type in new values. Each time you make a selection the cursor (?) moves to the next item. Note that the MAXIMUM SIM TIME and MAXIMUM DELTA T are usually entered in scientific (or exponential notation). For example to enter:

100ns	use	1E-7	or	100E-9
1ms	use	1E-3		

When you are finished the system will ask:

ARE THESE CORRECT (Y/N)?

If you press "N" the system will go through the entire list once again. If you press "Y" in response to the above question the system will then proceed with the next phase of the prologue.

If your circuit contains switches, then the system will ask:

ENTER SWITCH ON-RESISTANCE IN OHMS
DEFAULT = 1 OHM

Press RETURN to select an impedance of 1 OHM or type in any suitable value. Take care not to use a value that is more than 6 orders of magnitude different than other impedances connected to the switch nodes, as this may introduce roundoff errors.

MONITORING CURRENT, POWER & ENERGY DISSIPATION

When specifying the upper and lower traces it is possible to monitor current, power and energy or differential voltage by entering a string instead of the usual single node number. The format for this string is:

N1/N2/LETTER	0<N1<MAX NODE NO. 0<N2<MAX NODE NO. LETTER=V,I,P or E

For example to monitor the voltages between nodes 13 and 17 you would enter:

13/17/V

To monitor the current flowing into the resistance connected between the same two nodes you would enter:

13/17/I

To monitor the power flowing into that same resistance you would enter:

13/17/P

Power is calculated as the instantaneous product of the differential voltage and the current. To monitor the energy dissipated in the resistance you would enter:

13/17/E

In general the format and formulas are:

V=V(N1)-V(N2)
I=I
P=V*I

$$E=\int V*dt$$

Both the upper and lower traces may be so specified. Note that offset and scale factor should be correspondingly adjusted if you use this option. For example the offset parameter, when monitoring current, would be offset current and the scale factor units would be amperes instead of volts. Note also that the current, power and energy options are meaningful only if there exits a purely resistive impedance between the two nodes and neither node is the ground or zero node. Otherwise this technique does not produce meaningful results when any other type of impedance or source is connected across the two nodes. Of course, for differential voltages no such restrictions apply.

RESETTING CIRCUIT VARIABLES

The system will next ask:

ZERO INITIAL CONDITIONS (Y/N)?

If you press "Y" the system will set all node voltages and inductor currents to an initial value of zero. Otherwise it will not change their initial value. If this is the first time you have run a Transient Analysis on the circuit file since selecting the Transient Analysis option then these values will be zero anyway. However if this is your 2nd or later simulation (without returning to the ANALYZER menu) then the node voltage and inductor current variables still contain the last values calculated during the last simulation run. There will be occasions when you may want to do a simulation run just to set up initial conditions and then do another run without re-setting the variables. This option allows you to do so by pressing "N".

SETTING INITIAL CONDITIONS

This option begins with a menu:

1:SET INITIAL NODE VOLTAGES

2:SET INITIAL INDUCTOR CURRENTS

3:CONTINUE PROLOGUE

If you do not wish to alter the initial conditions simply press "3" and the system skips to the display mode selection.

If you wish to alter the initial node voltages press "1" and the system will display the initial voltages for each of the nodes in the network.

At the bottom of the screen the following message will appear:

PRESS E TO EDIT A VALUE OR Q TO QUIT

To alter any initial voltage simply press "E" and the system will print the query:

ENTER THE ITEM NO?

Simply enter the number of the node whose voltage you wish to change and press (RETURN). Then the system will ask:

ENTER THE NEW VALUE

Simply type in the desired initial voltage and press (RETURN). Following this last entry the system will re-display each node number and its initial voltage. When you are finished entering the desired initial node voltage press "Q" and control passes to the Initial Conditions menu. From here you may continue the prologue with "3" or set initial inductor currents with "2".

Setting initial inductor currents works exactly the same way. In order to tell the inductors apart they will be displayed on the screen labeled 1-40. The 1st inductor is the 1st inductor encountered on the Netlist, the 2nd is the 2nd and so on. Remember each transformer adds 2 inductors to the list, first the series and then the parallel inductance shown in the model.

WAVEFORM DUMP OPTION

Following the Initial Conditions Option the system will request:

DUMP NODE WAVEFORM TO USER FILE (Y/N)?

As explained in the ANALYZER section, a user may not only create a unique voltage waveform to be used as a driving source, he may also capture any node's voltage waveform created during a simulation and save it in a user file as well. This option is selected by responding "Y" to the above query. Pressing "N" bypasses this option and proceeds to the DISPLAY MODE SECTION.

If the user presses "Y" then the system will respond with:

ENTER THE NODE # TO DUMP

The user then types in the node # whose waveform is to be saved in the user file. The system then responds with:

ENTER FILE # TO DUMP TO (0-9)

Since there can be 10 different user files the user enters 0 to 9 and presses (RETURN). Following this last entry the prologue continues with the DISPLAY MODE SECTION.

There are several important facts to remember about user files:

1. Each user file is stored on the data diskette and consumes 15 to 20K bytes of diskette space.

2. Only one user file may be used as a source during a simulation.

3. A simulation may be run on a network which is both receiving a user waveform from a user source and dumping another waveform to another user file, provided they are different file numbers.

4. The TMAX assummed for a waveform to be saved is equal to the TMAX for the simulation.

5. If there is insufficient storage space on the data diskette the message

   DISK FULL
   ABORT DUMP

   will appear on the screen and the simulation will continue, bypassing the waveform dump.

DISPLAY MODE SELECTION

This portion begins with the prompt:

SELECT DISPLAY MODE

1:CRT DISPLAY ONLY
2:PRINTER PLOT
3:TABLE OF VOLTAGES

If you press "1" then the Transient Analysis results will be graphed directly on your CRT and only there. If you press "2" then the results will appear not only on your CRT but will also be sent to your printer in the form of a printer plot. Selecting "2" also requires that you respond to the query:

ENTER DESIRED STEPPING RATE.

This is the time interval that subsequent printer plot points will be incremented on. Generally speaking this number should be 0.1% to 1.0% of the TMAX value. If you wish to run a very long simulation with very small time increments the printer plot is a useful way of stretching the scale of what's shown on the CRT.

For example suppose you had a pulse amplifier circuit, driven by a voltage waveform of period 10MHZ. If you set TMAX at 10 micro-seconds and DELTA T at 10ns, the CRT waveform will be inadequate to show the detail. However you could select a 10ns stepping rate for printer plotter and get an "expanded scale". Be aware that, by definition, this technique will use a lot of paper. In this case the printer plot would be:

10000ns / 10ns

:

1000 lines long
(about 16 pages)

When you make this last selection the system will printout the plot header, draw the Transient Analysis grids and proceed with the actual simulation

DISPLAY MODE SELECTION

Selecting "3" from the Display menu will allow you to printout a tabular list of node voltages. This mode is used when you want to know the voltage on a large number of circuit nodes. In this way, up to 12 nodes can be monitored during a simulation. This option requires you to specify the decimal format of each column of node voltages. It begins with:

> ENTER THE MAXIMUM # OF DIGITS TO THE LEFT OF THE DECIMAL POINT.

If for example the system was expected to generate voltages less than one hundred volts you would enter 2. Then the system asks:

> ENTER THE MAXIMUM # OF DIGITS TO THE RIGHT OF THE DECIMAL POINT.

Here you simply indicate the precision you want to see in the printout. For example if you wanted each printed voltage to be shown to the nearest milli-volt you would enter 3, to the nearest tenth of a volt you would enter 1 and so on.

When you answer this last question the system will calculate the maximum number of node voltages that can be printed out on an 80 column printer and print the message:

> THIS ALLOWS A MAXIMUM OF XX NODES TO BE PRINTED OUT OK (Y/N)?

Pressing "Y" signifies your acceptance. Pressing "N" will allow you to respecify the left and right hand digit count and the system will repeat the procedure until the desired set is found. Pressing "Y" causes the system to enter the Table node selection process. It begins by printing this message on the screen:

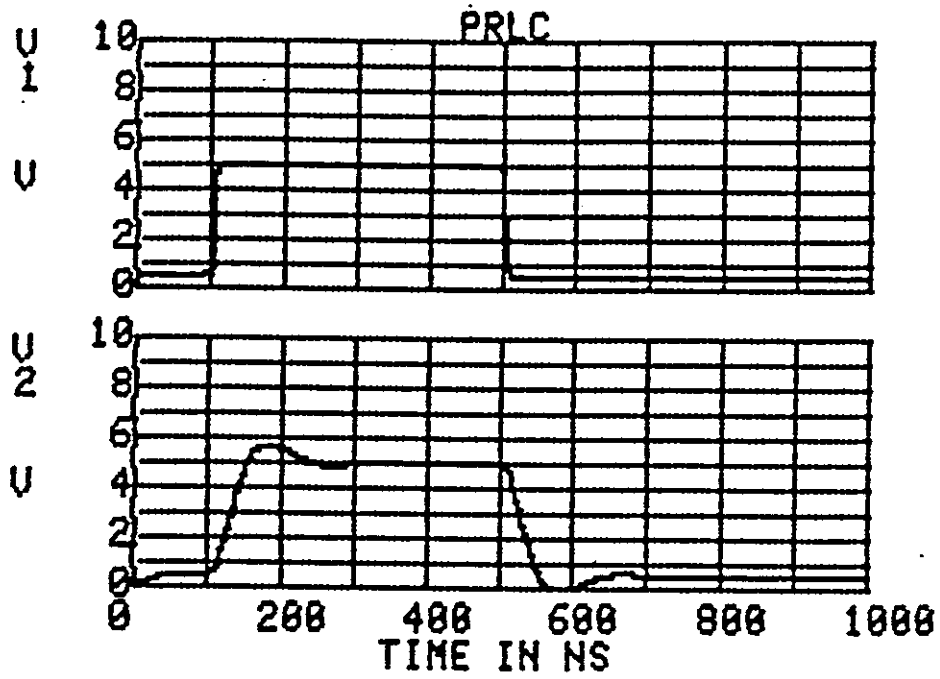
> ENTER ZERO TO TERMINATE THE ENTRY PROCESS.
>
> ENTER PRINTOUT NODE #1?

Here the user enters the number of the 1st node to be printed out. Then the user enters the 2nd and so on until all of the XX printout positions available to you with the format you have chosen are used or until you get tired of entering. In the latter case you simply enter zero to terminate the entry process.

When finished the system prints out the TABLE PLOT header and proceeds with the simulation.

THE TRANSIENT ANALYSIS DISPLAY

When a Transient Analysis is run on the PRLC file the results on the video display look like this:



There are 2 grid panels, one for each node monitored. Each panel is divided into a grid of 10 vertical divisions by 10 horizontal divisions. The horizontal represents time, with each division representing one tenth of TMAX.

IV TRANSIENT ANALYSIS

THE TRANSIENT ANALYSIS DISPLAY

The vertical direction represents voltage at the scale selected by the user. The top panel monitors the 1st node selected and the bottom panel monitors the 2nd node selected. Each panel shows the node # and units:

KV =	KILOVOLTS	=	10^{3}
V =	VOLTS	=	10^{0}
MV =	MILLIVOLTS	=	10^{-3}
UV =	MICROVOLTS	=	10^{-6}
NV =	NANVOLTS	=	10^{-9}

If you are monitoring current, power and energy the "V" will be replaced with A, W, or J respectively to represent amperes, watts or joules.

Similarly the time scale units are:

KS =	KILOSECONDS =		10^{3}
S =	SECONDS	=	10^{0}
MS =	MILLSECONDS =		10^{-3}
US =	MICROSECONDS=		10^{-6}
NS =	NANOSECONDS =		10^{-9}
PS =	PICOSECONDS =		10^{-12}
FS =	FEMTOSECONDS=		10^{-15}

The offset voltage is used in the same way as the vertical deflection knob on an oscilloscope; to move the waveform up or down on the screen to view (usually at a lower scale factor) some part of the waveform. For example, to look at a signal with a 300 volt average DC value you might use an offset of 300 volts and a scale factor of 1v/div. Without the offset feature you would be forced to use a scale factor of at least 30 volts/div and would get a highly compressed view of the waveform.

Following the selection of display mode the system loads and runs the actual simulation routine.

The simulation proceeds from Time = 0 to Time = TMAX with the results displayed as you have selected.

Note that the simulation can be stopped at any time by pressing the "Q" key. Just hold down the "Q" key until the message "PRESS ANY KEY" (or on the IBM the "SAVE GRAPH" message) appears.

EPILOG OPTIONS

Following completion of the simulation (or pressing the Q key) the system prints the message:

PRESS ANY KEY

Press any key and the system displays the Epilog Menu.

EPILOG OPTIONS

1. SAVE GRAPH ON DATA DISK.
2. ANOTHER RUN.
3. PRINTOUT ANALYSIS LIMITS.
4. RETURN TO ANALYZER MENU
5. SILENTYPE DUMP. (APPLE ONLY)
6. MX-80 DUMP. (APPLE ONLY)
7. GRAPHICS CARD DUMP (APPLE ONLY)

Selecting option 1 saves the graph on your data disk in binary form (for later retrieval and dumping to a printer).

The file is saved under the following name:

CIRCUIT NAME + "TIME GRAPH" (APPLE)
CIRCUIT NAME + "TGR" (IBM)

Selecting option 2 allows you to make another analysis run.

Selecting option 3 causes the analysis limits to be printed out on your printer.

Selecting option 4 causes control to pass to the Analyzer Menu.

Option 5, 6 & 7 works exactly the same ways as described in the Designer section and are available on the APPLE II only. Printer dumps of the graphs are available on the IBM through use of the SHIFT/PRT SC command.

PRINTER PLOT EXAMPLE

If you selected the printer plot option for the PRLC analysis the resulting plot would look like this:

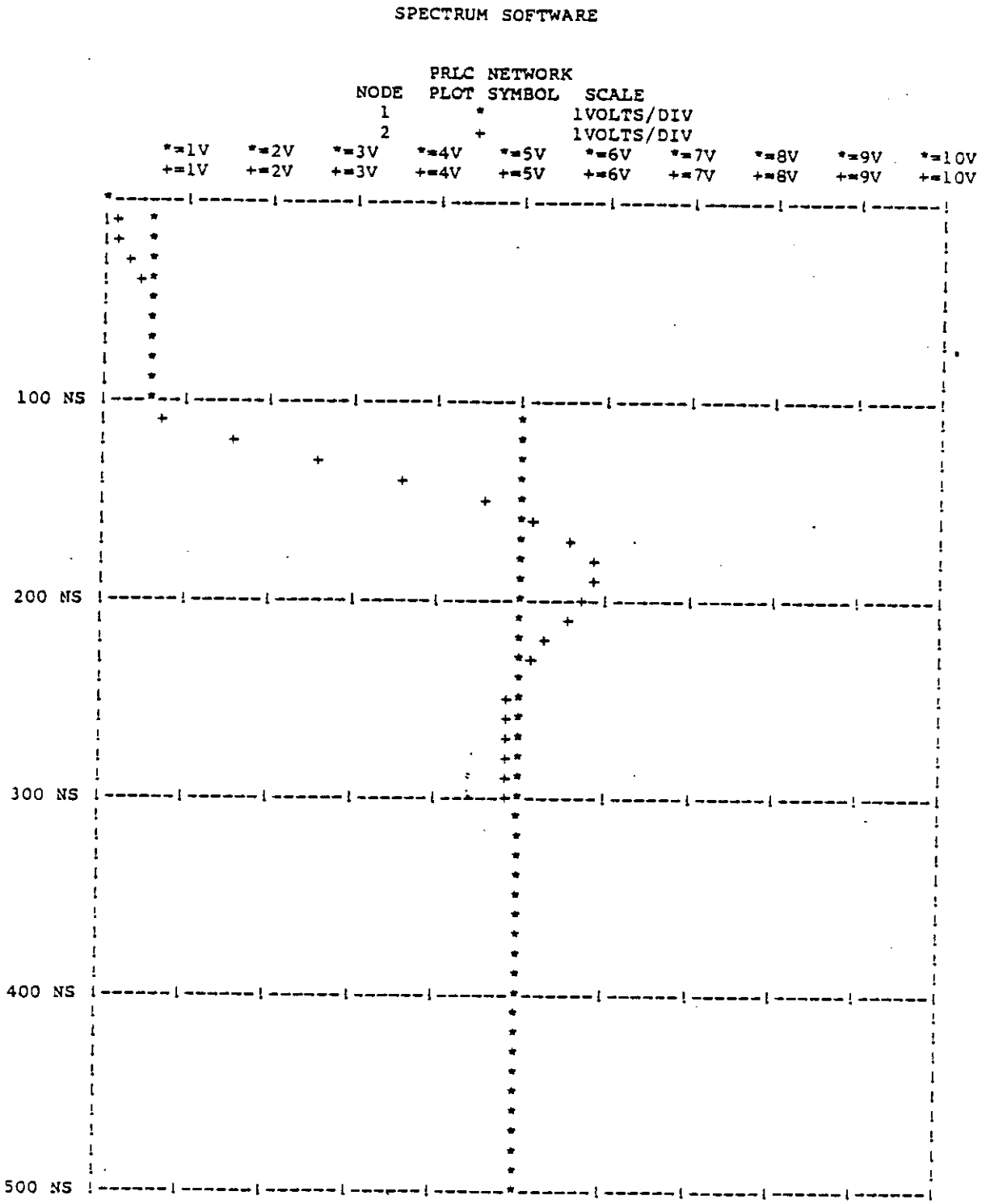


TABLE OF VOLTAGES EXAMPLES

If you selected the TABLE OF VOLTAGES option for the PRLC analysis the result would look like this:

SPECTRUM SOFTWARE

PRLC NETWORK
NODE VOLTAGES

TIME NS	V1	V2	V3	V1	V2	V3
0.0	0.5000	0.0001	0.0000	0.5000	0.0001	0.0000
0.2	0.5000	0.0002	0.0000	0.5000	0.0002	0.0000
5.2	0.5000	0.0411	0.0000	0.5000	0.0411	0.0000
10.2	0.5000	0.0923	0.0000	0.5000	0.0923	0.0000
15.2	0.5000	0.1495	0.0000	0.5000	0.1495	0.0000
20.2	0.5000	0.2092	0.0000	0.5000	0.2092	0.0000
25.2	0.5000	0.2687	0.0000	0.5000	0.2687	0.0000
30.2	0.5000	0.3255	0.0000	0.5000	0.3255	0.0000
35.2	0.5000	0.3780	0.0000	0.5000	0.3780	0.0000
40.2	0.5000	0.4248	0.0000	0.5000	0.4248	0.0000
45.2	0.5000	0.4653	0.0000	0.5000	0.4653	0.0000
50.2	0.5000	0.4990	0.0000	0.5000	0.4990	0.0000
55.2	0.5000	0.5261	0.0000	0.5000	0.5261	0.0000
60.2	0.5000	0.5467	0.0000	0.5000	0.5467	0.0000
65.2	0.5000	0.5613	0.0000	0.5000	0.5613	0.0000
70.2	0.5000	0.5705	0.0000	0.5000	0.5705	0.0000
75.2	0.5000	0.5751	0.0000	0.5000	0.5751	0.0000
80.2	0.5000	0.5757	0.0000	0.5000	0.5757	0.0000
85.2	0.5000	0.5732	0.0000	0.5000	0.5732	0.0000
90.2	0.5000	0.5683	0.0000	0.5000	0.5683	0.0000
95.2	0.5000	0.5616	0.0000	0.5000	0.5616	0.0000
100.2	0.6125	0.5583	0.0000	0.6125	0.5583	0.0000
105.2	2.8625	0.6478	0.0000	2.8625	0.6478	0.0000
105.6	3.0625	0.6478	0.0000	3.0625	0.6478	0.0000
106.1	3.2625	0.6487	0.0000	3.2625	0.6487	0.0000
106.5	3.4625	0.6508	0.0000	3.4625	0.6508	0.0000
107.0	3.6625	0.6539	0.0000	3.6625	0.6539	0.0000
107.4	3.8625	0.6583	0.0000	3.8625	0.6583	0.0000
107.9	4.0625	0.6639	0.0000	4.0625	0.6639	0.0000
108.3	4.2625	0.6708	0.0000	4.2625	0.6708	0.0000
108.8	4.4625	0.6790	0.0000	4.4625	0.6790	0.0000
109.2	4.6625	0.6887	0.0000	4.6625	0.6887	0.0000
109.6	4.8625	0.6997	0.0000	4.8625	0.6997	0.0000
110.1	5.0000	0.7123	0.0000	5.0000	0.7123	0.0000
110.7	5.0000	0.7347	0.0000	5.0000	0.7347	0.0000
115.7	4.9999	1.1923	0.0000	4.9999	1.1923	0.0000
117.9	4.9999	1.3651	0.0000	4.9999	1.3651	0.0000
120.0	4.9999	1.5920	0.0000	4.9999	1.5920	0.0000

V AC ANALYSIS

Option 4 on the ANALYZER main menu is used to perform AC or frequency analysis. This type of analysis plots the gain and phase delay of an output node's voltage vs an input node's voltage, where the user specifies which node is the input and which is the output. This type of analysis is also know as:

- Linear Analysis
- Bode Analysis
- Frequency Domain Analysis

To perform this type of analysis, begin at the ANALYZER main menu and first create or retrieve a circuit file using options 1 or 2 from that menu. Then select Option 4 from the menu. As in this case of Transient Analysis the system runs through the prologue first to determine the analysis limits.

To illustrate the use of this module go to the ANALYZER main menu and, using Option 1, retrieve the PRLC file. Then select option 4 for the AC ANALYSIS.

AC ANALYSIS PROLOGUE

The prologue begins with a display that looks like this:

ANALYSIS LIMITS

PRESS (RETURN) TO ACCEPT DEFAULT VALUES OR TYPE DESIRED VALUE AND PRESS (RETURN).

LOWEST FREQUENCY	1E5
HIGHEST FREQUENCY	1E8
LOWEST GAIN	.1
HIGHEST GAIN	10
INPUT NODE NUMBER	1
OUTPUT NODE NUMBER	2
MINIMUM ACCURACY (%)	5
HIGHEST PHASE SHIFT	0
LOWEST PHASE SHIFT	-360

As in the Transient Analysis prologue the system positions the cursor at each successive item, prints a question mark and waits for your entry. Pressing (RETURN) signifies acceptance of the printed value, or you may type in a new value.

For our example enter the analysis limits listed above.

AC ANALYSIS PROLOGUE

The lowest and highest frequency tells the system the frequency range to scan over. The lowest and highest gain and phase shift numbers are used to scale the graph vertically.

When the analysis begins the system will apply a 1 volt signal to the node specified as the input, step its frequency from LOW to HIGH calculating the voltage and phase shift of the output node at each frequency and plot the relative gain and phase delay between input and output.

At each iteration if the change in gain is less than a critical amount the system will increase the frequency step. Conversely, if the change is too large the system will decrease the frequency step. The MINIMUM ACCURACY parameter directly controls the critical amount. By lowering it you obtain a more accurate graph, but it takes longer since there will be more and smaller frequency steps. The converse is also true.

When you have completed your selection of analysis limits, press "Y" and the system will ask:

INCLUDE MINOR GRIDS (Y/N)?

Pressing Y forces the system to include grids at each sub-cycle of each power of 10 (eg. at .01, .02, .03, ... etc.). Pressing "N" causes the display to include only grids at each power of 10 (eg. at gain of .01, .1, 1, 10 etc).

The system next asks:

GRID DOT SPACING (0-2)?

Enter 0 and the grids are plotted as solid lines. Enter 1 or 2 and the grids are plotted as dotted lines. The latter takes longer but produces an easier to read display.

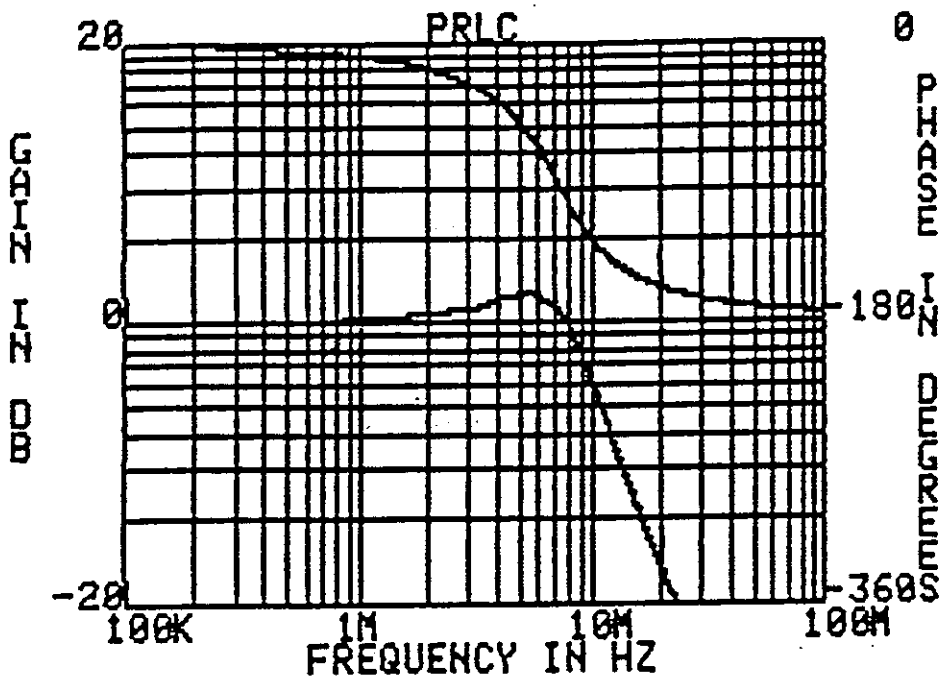
Finally the system asks:

HARD COPY (Y/N)?

If you press "Y" the system will generate a printed table showing the frequency, gain and phase at each step of the subsequent analysis. Pressing "N" will yield only the CRT display.

AC ANALYSIS DISPLAY

The AC analysis for the PRLC circuit looks like this:




```
FREQUENCY =  100000000
GAIN      =  5.08146E-3 ANG = -176.34
SLOPE     = -12.0777988 DB/OCTAVE
PEAK GAIN =  1.61799919 AT F=6450000
```

AC ANALYSIS DISPLAY

On the screen are plotted both gain and phase. Gain is plotted in units of DB using the scale on the left. Phase is plotted in degrees using the scale on the right.

In the bottom panel are shown:

LINE 1: The current frequency
LINE 2: The current gain and angle calculated
LINE 3: The current slope in DB/OCTAVE
LINE 4: The peak gain so far encountered (in the current run)

PRINTER OPTION

If you selected the Hard Copy option the system would have generated a result that looks like this:

SPECTRUM SOFTWARE
MICRO-CAP
FREQUENCY ANALYSIS
FOR
PRLC CIRCUIT

FREQUENCY	GAIN(RATIO)	GAIN(DB)	ANGLE(DEGREES)	SLOPE(DB/OCTAVE)
100000	1.00009843	8.54917681E-04	-.72	0
150000	1.00024647	2.14056315E-03	-1.08	2.19782545E-03
250000	1.00072024	6.25364406E-03	-1.8	5.58110872E-03
450000.001	1.00237879	.0206373453	-3.25	.0169619737
850000.001	1.0085435	.0738927326	-6.18	.0580416236
1650000	1.03227818	.275934927	-12.36	.211135532
3250000	1.12273415	1.00553866	-27.29	.746036142
6450000.01	1.20475839	1.61799919	-77.56	.619360565
8050000.01	.952906239	-.418996591	-105.43	-6.371792
9650000.01	.678361225	-3.37077968	-124.65	-11.2861562
11250000	.485450115	-6.27710784	-136.66	-13.1315453
12850000	.360085584	-8.87188531	-144.45	-13.5255007
14450000	.276906557	-11.1533352	-149.81	-13.475692
16050000	.219506862	-13.171038	-153.72	-13.3178356
17650000	.178361834	-14.9739614	-156.7	-13.1509165
19250000	.147882991	-16.6016355	-159.04	-13.0016029
20850000	.124671563	-18.0846519	-160.93	-12.8746428
22450000	.106578221	-19.4466307	-162.5	-12.7683837
25650000	.0805627913	-21.8773099	-164.95	-12.6437605
28850000	.0630931084	-24.0003615	-166.78	-12.5170709
32050000	.0507809545	-25.8859829	-168.2	-12.4255918
35250000	.0417700969	-27.5826904	-169.34	-12.3577648
38450000	.0349727512	-29.1254041	-170.27	-12.3062342
41650000	.0297163036	-30.5401043	-171.05	-12.2662332
48050000	.0222315843	-33.0605918	-172.29	-12.2223271
54450000	.0172626957	-35.2578278	-173.22	-12.1800962
60850000	.0137943921	-37.2058487	-173.94	-12.1510579
67250000	.0112770829	-38.9560646	-174.53	-12.1302482
73650000	9.39189012E-03	-40.54494	-175.01	-12.1148315
80050000	7.94335173E-03	-41.9999242	-175.42	-12.1030951
86450000	6.80618537E-03	-43.3419246	-175.76	-12.093955
99250000	5.15878851E-03	-45.7490456	-176.31	-12.0838716
100000000	5.08146311E-03	-45.8802245	-176.34	-12.077988

EPILOG OPTIONS

Following completion of the simulation (or pressing the Q key) the system prints the message:

PRESS ANY KEY

Press any key and the system displays the Epilog Menu.

EPILOG OPTIONS

1. SAVE GRAPH ON DATA DISK.
2. ANOTHER RUN.
3. PRINTOUT ANALYSIS LIMITS.
4. RETURN TO ANALYZER MENU.
5. SILENTYPE DUMP (APPLE ONLY).
6. MX-80 DUMP. (APPLE ONLY).
7. GRAPHICS CARD DUMP (APPLE ONLY).

Selecting option 1 saves the graph on your data disk in binary form (for later retrieval and dumping to a printer).

The file is saved under the following name:

CIRCUIT NAME + "FREQ GRAPH" (APPLE)
CIRCUIT NAME + "EGR" (IBM)

Selecting option 2 allows you to make another analysis run.

Selecting option 3 causes the analysis limits to be printed out on your printer.

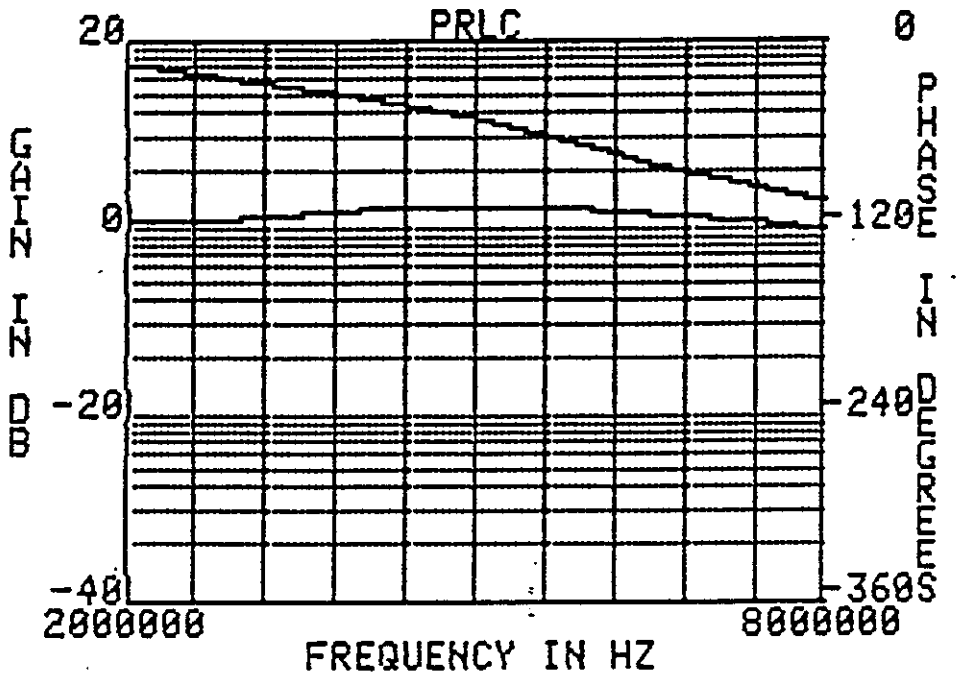
Selecting option 4 causes control to pass to the Analyzer Menu.

Option 5, 6 & 7 works exactly the same ways as described in the Designer section and are available on the APPLE II only. Printer dumps of the graphs are available on the IBM through use of the SHIFT PRT SC key.

LINEAR SWEEP OPTION

When you enter the upper and lower frequency limits, a linear sweep of frequency may be obtained by appending "L" to the frequency. For example 1E6L and 1E7L as frequency limits for this example would cause the system to linearly sweep the frequency from 1MHZ to 10MHZ and plot the results on a linear frequency scale.

A typical linear frequency sweep produces a display that looks like this:



VI DC ANALYSIS

This analysis mode is selected by pressing "5" from the ANALYZER main menu. As in the other analysis modes, the user must select the analysis limits. These limits are:

MAXIMUM INPUT VOLTAGE
MAXIMUM OUTPUT VOLTAGE
VOLTAGE STEP
INPUT PIN #
OUTPUT PIN #
NO. OF ITERATIONS
STARTING INPUT VOLTAGE.

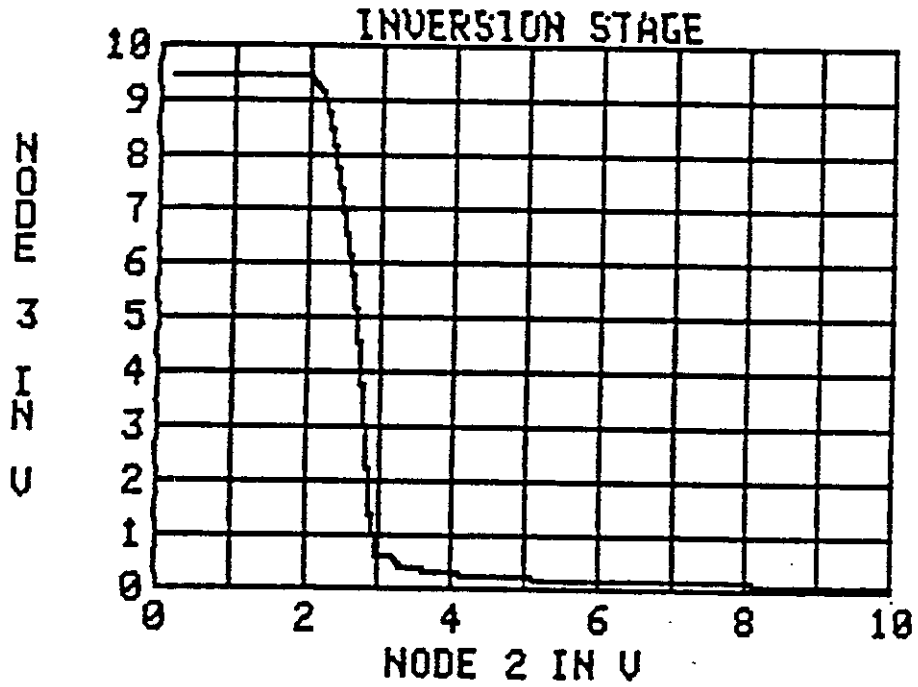
In this mode the computer plots the DC voltage on the user specified output node vs the DC voltage on the user specified input node, creating a DC Transfer Characteristic. The analysis begins with the voltage on the input pin set to the STARTING INPUT VOLTAGE. The output node voltage is calculated and plotted. The input nodes' voltage is then increased by the VOLTAGE STEP and the output voltage is calculated and plotted. At each step the system makes as many iterations as the user has specified with the NO. OF ITERATIONS parameter. More iterations produce greater accuracy but increase the analysis time. Generally the choice of iterations should be between 2 and 5, with more iterations required as the expected DC gain (slope of the curve) of the circuit increases. Following selection of these parameters, the system asks:

HARD COPY (Y/N)?

If you press "Y" the system will create a printed list of the input voltage, output voltage and DC gain at each step of the analysis.

DC ANALYSIS DISPLAY

The analysis results are displayed as a voltage graph. A typical analysis looks like this:



Output voltage is plotted on the vertical axis (ordinate) and input voltage is plotted on the horizontal axis (abcissa).

During the analysis, the "text window" below the graph displays:

- Current Input Voltage
- Current Output Voltage
- Current Slope
- Peak Output Voltage (largest value encountered)
- Peak Slope (largest value encountered)

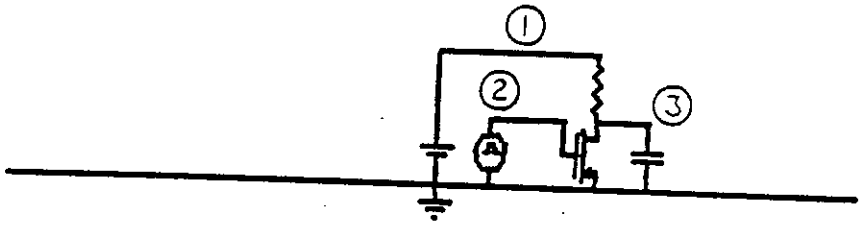
When the analysis is complete, a flashing cursor will appear in the text window. As in the other analysis modes, pressing any key will clear the screen and present you with the opportunity to save the graph in a disk file, optionally dump to Silentype (Apple) and to run another analysis.

DC ANALYSIS EXAMPLE

To illustrate the use of this analysis mode, run the program and get the ANALYZER menu up. Select option 1 and recall the circuit file:

MOS INVERTER-R

This circuit is a simple MOS transistor-resistor inverting stage. It looks like this:



The input node number is 2, the output node number is 3.

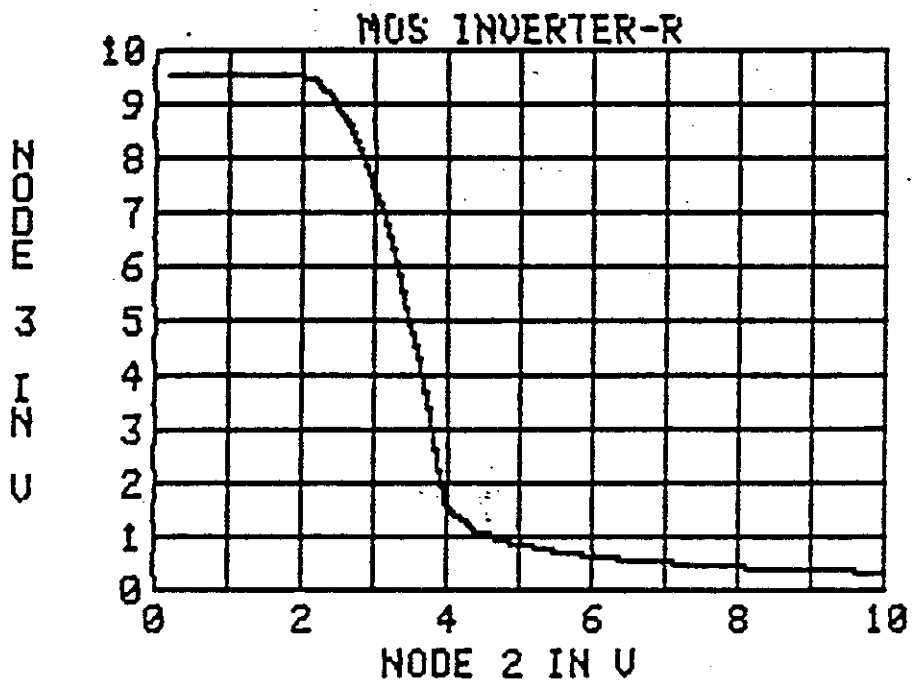
DC ANALYSIS EXAMPLE

From the ANALYZERS' menu select the DC ANALYSIS option (#5) and when the prologue comes up enter these limits.

MAXIMUM INPUT VOLTAGE	10
MAXIMUM OUTPUT VOLTAGE	10
VOLTAGE STEP	0.1
INPUT NODE #	2
OUTPUT NODE #	3
NO. OF INTERATIONS	2
STARTING INPUT VOLTAGE	0

Select the printer list by pressing "Y" to the "HARDCOPY (Y/N)? Query.

These selections produce an analysis that looks like this:



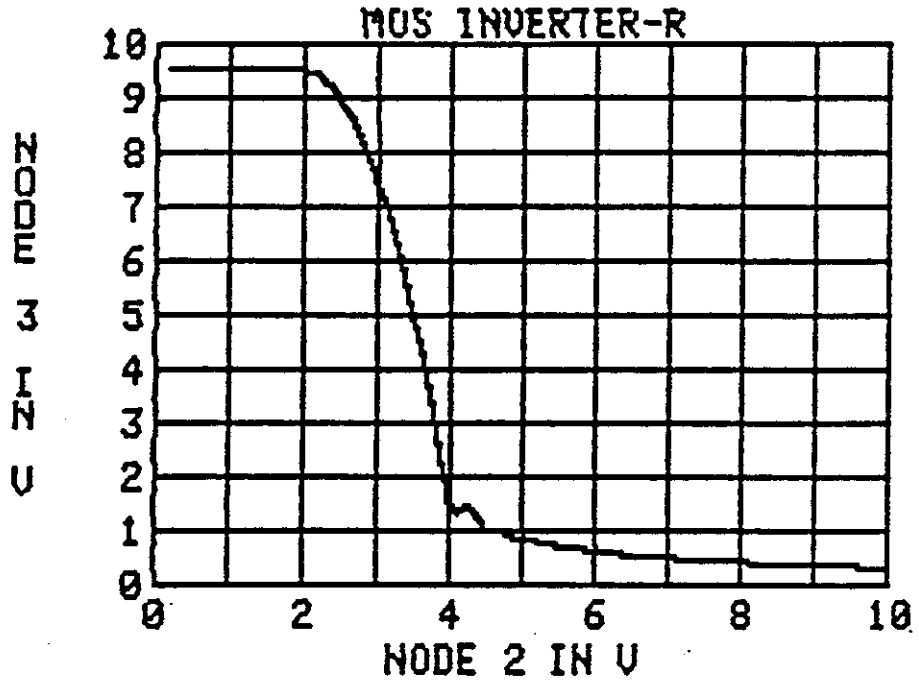
DC ANALYSIS PRINTER OPTION

The printer list looks like this:

SPECTRUM SOFTWARE
MICRO-CAP
DC TRANSFER CHARACTERISTIC ANALYSIS
FOR
MOS INVERTER-R CIRCUIT

INPUT VOLTAGE	OUTPUT VOLTAGE	SLOPE
.1	9.49810038	0
.2	9.49810038	0
.3	9.49810038	0
.4	9.49810038	0
.5	9.49810038	0
.6	9.49810038	0
.7	9.49810038	0
.8	9.49810038	0
.9	9.49810038	0
1	9.49810038	0
1.1	9.49810038	0
1.2	9.49810038	0
1.3	9.49810038	0
1.4	9.49810038	0
1.5	9.49810038	0
1.6	9.49810038	0
1.7	9.49810038	0
1.8	9.49810038	0
1.9	9.49810038	0
2	9.47810437	.2
2.1	9.41811739	.6
2.2	9.31813547	1
2.3	9.17816276	1.4
2.4	8.99819786	1.8
2.5	8.77824074	2.2
2.6	8.51829144	2.599
2.7	8.21834993	2.999
2.8	7.87841622	3.399
2.9	7.49849031	3.799
3	7.07857219	4.199
3.1	6.61866188	4.599
3.2	6.11875936	4.999
3.3	5.57886465	5.399
3.4	4.99897773	5.799
3.5	4.37909861	6.199
3.6	3.71922729	6.599
3.69999999	3.01936377	6.999
3.79999999	2.27950804	7.399
3.89999999	1.62837558	6.511
3.99999999	1.39991278	2.285
4.09999999	1.37151209	.284
4.19999999	1.26172091	1.098
4.29999999	1.1371593	1.246
4.39999999	1.06859198	.686
4.49999999	1.01553922	.531
4.59999999	.962494908	.53
4.69999999	.916100795	.464
4.79999999	.875681016	.404
4.89999999	.839113117	.366
4.99999999	.805878919	.332
5.09999999	.775572222	.303
5.19999999	.747757621	.278
5.29999999	.722104759	.257
5.39999999		
5.49999999		

To illustrate the effect of changing the number of iterations, re-run the analysis with 1 iteration specified. The results look like this:



Notice the "wrinkle" in the lower part of the curve. In this example one iteration was insufficient to produce convergence in this region of voltage. In general, convergence is most critical in the region of maximum DC gain and it is this region which determines the number of iterations needed to produce accurate results.

The accuracy of the results are also affected by the selection of voltage step. Generally a step of 1 to 2% of the maximum input voltage is a suitable choice, but higher gain circuits may require a smaller value. Extremely high gain circuits will require extremely small voltage steps. The smaller the step the longer the analysis will take. For this reason users may wish to by pass the relatively uninteresting pre-switching point region by specifying a non-zero STARTING INPUT VOLTAGE.

STOPPING AN ANALYSIS

Once in progress, an analysis will continue until the:

1. The input voltage equals the maximum specified.
2. The user presses "Q".

Pressing "Q" causes the analysis to terminate and produces the usual flashing cursor but does not clear the screen. Pressing any other key clears the screen and proceeds with the usual epilog options.

VII STANDARD COMPONENT MODELS

In the succeeding pages are defined the Standard Component Models for:

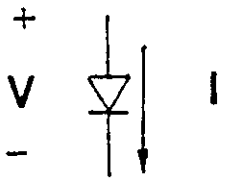
COMPONENT	PAGE
DIODES	7-2
BIPOLAR TRANSISTORS	7-5
OPAMPS	7-8
TRANSFORMERS	7-11
SINUSODIAL VOLTAGE SOURCES	7-13
PROGRAMMABLE VOLTAGE WAVEFORMS	7-14
MOS TRANSISTORS	7-15
POLYNOMIAL SOURCES	7-18

In addition the models for the following components are included:

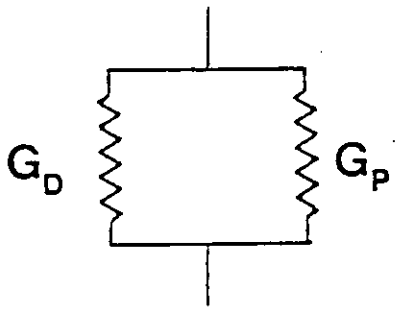
RESISTOR	7-19
INDUCTOR	7-19
CAPACITOR	7-19
BATTERY	7-20
SWITCHS	7-21
USER SOURCE	7-24

DIODE MODELS
FOR DC AND TRANSIENT ANALYSIS

SYMBOL:



MODEL:



EQUATIONS: G=GD+GP

$$GD=\begin{cases} 1/RZ & :V<=-VZ \\ \frac{1}{VT}*IO*(EXP(V/VT) & :-VZ<V<VO \\ 1/RF & :V>=VO \end{cases}$$

VO=VT*LN(VT/(RF*IO))

GP=1/RP

DIODE MODEL
FOR DC AND TRANSIENT ANALYSIS

PARAMETERS:

	NAME	SYMBOL	TYPICAL VALUES
1.	SATURATION CURRENT	IO	1E-13 to 1E-15
2.	ZENER VOLTAGE	VZ	5V to 300V
3.	ZENER RESISTANCE	RZ	1 to 1000
4.	SERIES RESISTANCE	RF	1 to 1000
5.	VT TERM (VT=K*T/Q)	VT	.026
6.	PARALLEL RESISTANCE	RP	100 to 1E6

NOTES:

1. RF is the limiting or minimum forward dynamic resistance of the diode. When the dynamic resistance of the ideal diode model drops below RF, the model effectively replaces the ideal diode with a resistance of RF.

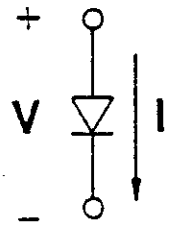
2. The total resistance of the complete diode model is the parallel combination of RF and RP.

3. RP is included for cases where "numerical isolation" might occur. A reversed-biased diode has an impedance much greater than the numerical precision of the computer and is effectively infinite. Unless the diode has a numerically finite impedance to another part of the circuit, a singularity will occur in the matrix inversion and no solution will be possible. RP overcomes the limitation.

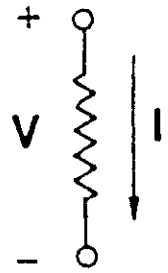
VII STANDARD COMPONENT MODELS

DIODE MODEL
FOR AC ANALYSIS

SYMBOL:



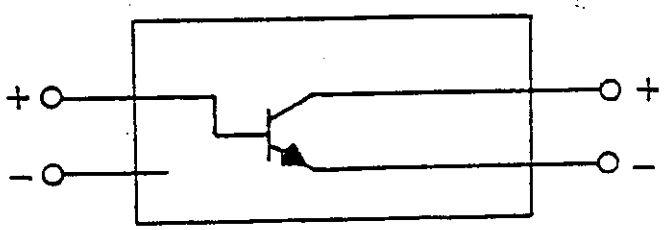
MODEL:



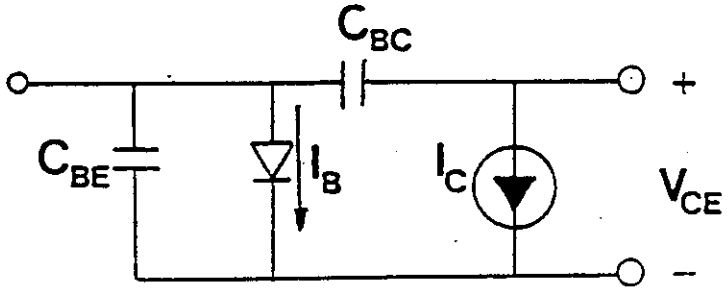
EQUATIONS: I=GF*V

BIPOLAR TRANSISTOR MODELS FOR DC AND TRANSIENT ANALYSIS

SYMBOL:
(TWO PORT)



MODEL:



EQUATIONS:

$$IC = \begin{cases} 0 & : IB <= 0 \\ \beta * IB & : VCE > RSAT * IC \\ VCE/RSAT & : VCE <= RSAT * IC \end{cases}$$

BIPOLAR TRANSISTOR MODEL
FOR DC AND TRANSIENT ANALYSIS

PARAMETERS:

	NAME	SYMBOL	TYPICAL VALUES
1.	BETA (HFE)	B	20-200
2.	BASE-EMITTER DIODE TYPE #	-	0-4
3.	F-TAU=UNITY GAIN BANDWIDTH	FT	5E7-5E8
4.	COLLECTOR CURRENT (HFE,FT)	ICF	.1ma to 100ma
5.	SATURATION RESIST.	RSAT	.1 to 10
6.	CAPACITANCE B-E	CBE	1 pf to 1nf
7.	CAPACITANCE C-B	CBC	1 pf to 1nf

NOTES:

1. CBE is calculated by the program from the following equation:

   CBE = ICF/(2*FT*VT*PI) : PI = 3.1415

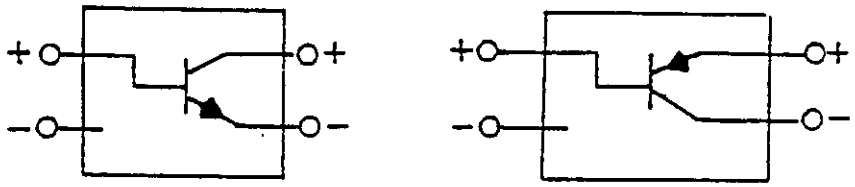
2. The BASE-EMITTER DIODE TYPE # is the Standard Diode type to be used in constructing the transistor model.

3. Polarity of both the diode and current source are reversed for PNP transistors.

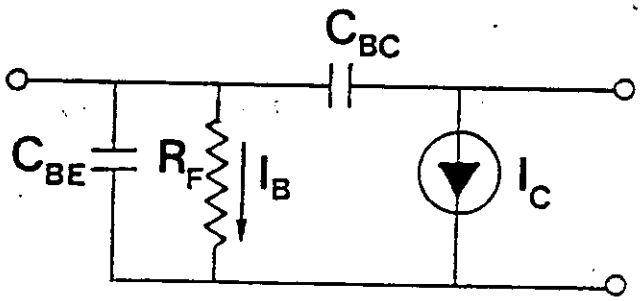
VII STANDARD COMPONENT MODELS

BIPOLAR TRANSISTOR MODEL FOR AC ANALYSIS

SYMBOL:



MODEL:



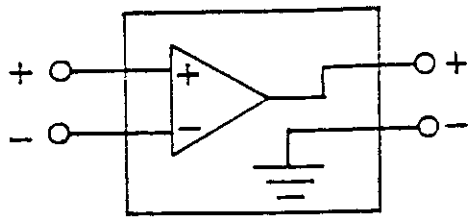
EQUATIONS: $IC = \beta * IB$

NOTES:

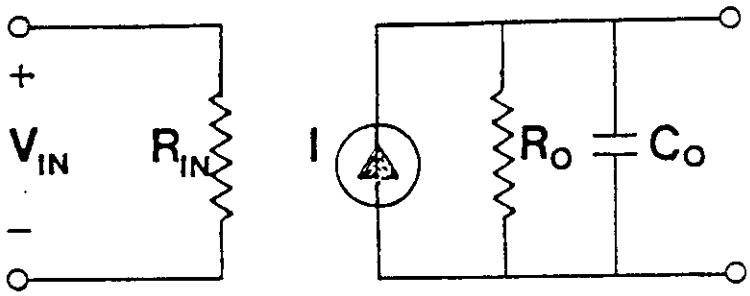
1. POLARITY IS IMPORTANT IN AC ANALYSIS ESPECIALLY IN COMPLIMENTARY CIRCUITS.

OPAMP MODEL FOR
DC AND TRANSIENT ANALYSIS

SYMBOL:



MODEL:



EQUATIONS:

$$I=\begin{cases} VMAX/RO & : VIN-VOFF >= VMAX/AO \\ AO*(VIN-VOFF)/RO & : -VMAX/AO < VIN-VOFF < +VMAX/AO \\ -VMAX/RO & : VIN-VOFF <= -VMAX/AO \end{cases}$$

OPAMP MODEL FOR
DC AND TRANSIENT ANALYSIS

PARAMETERS:

	NAME	SYMBOL	TYPICAL VALUES
1.	INPUT RESISTANCE	RI	1E4 to 1E8
2.	OPEN LOOP GAIN	AO	100 to 10E5
3.	OUTPUT RESISTANCE	RO	100 to 1E4
4.	INPUT OFFSET VOLTAGE	VOFF	.1MV TO 1MV
5.	MAXIMUM OUTPUT VOLT	VMAX	10V TO 30V
6.	OUTPUT CAPACITANCE	CO	100pf to 1000pf

NOTES:

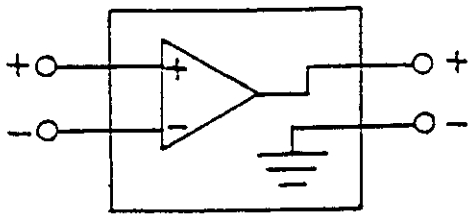
1. The parameter VMAX is the maximum voltage the output will rise to given an unloaded condition.

2. Most OPAMPS are designed for 2 power supply usage, typically +- 15 volts. For this example the VMAX parameter would normally be set to +30 volts and any input signal source would be connected on one side a +15 volt battery.

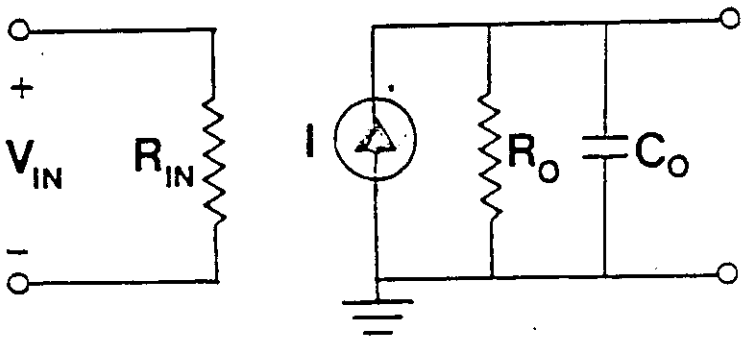
VII STANDARD COMPONENT MODELS

OPAMP MODEL FOR AC ANALYSIS

SYMBOL:

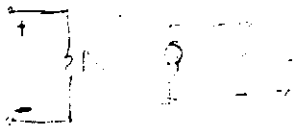


MODEL:



EQUATIONS: I=AO*VIN/RO

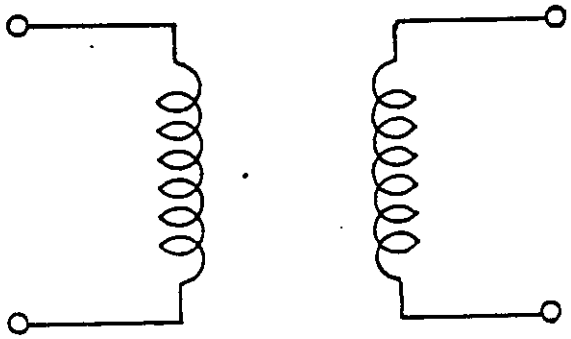
Termini di passaggi dei parametri:



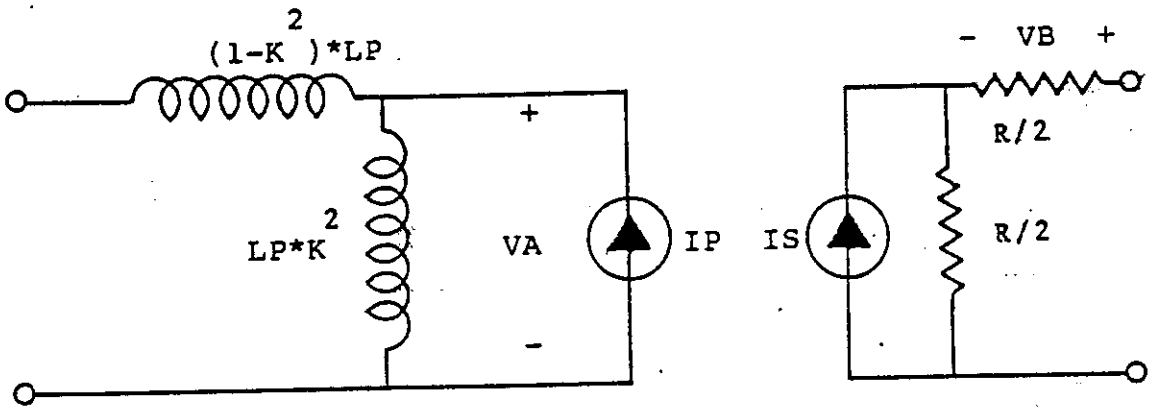
VII STANDARD COMPONENT MODELS

TRANSFORMER MODEL
FOR AC, DC AND TRANSIENT ANALYSIS

SYMBOL:



MODEL:



EQUATIONS: IP= 2*VB/R

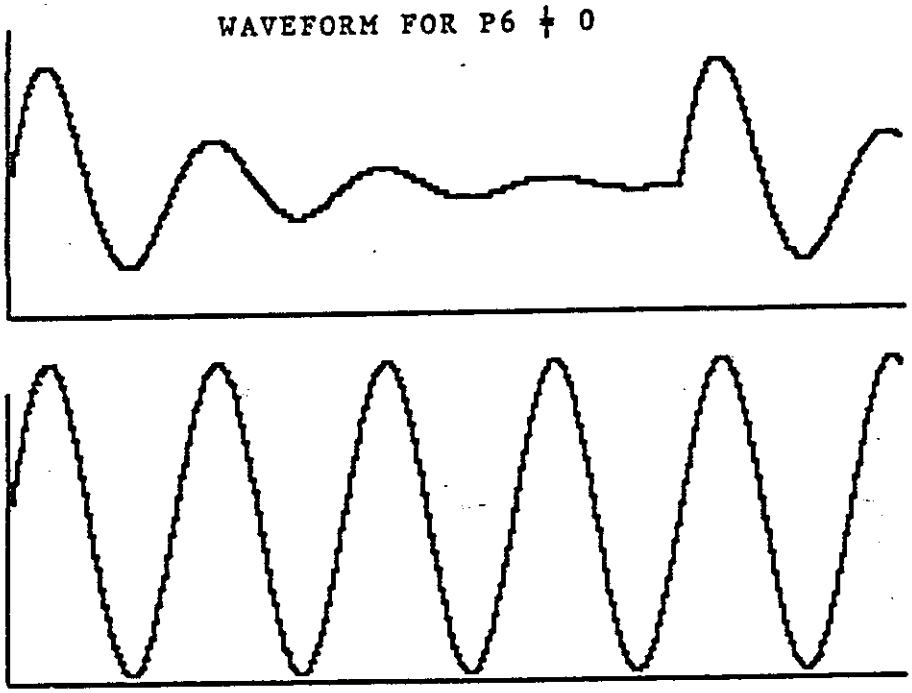
IS= 2*VA/R

TRANSFORMER MODEL
FOR AC, DC AND TRANSIENT ANALYSIS

PARAMETERS:

	NAME	SYMBOL	TYPICAL VALUES
1.	INPUT SELF INDUCTANCE	LP	1E-3 to 100H
2.	CURRENT GAIN (TURNS RATIO)	N	.01 to 100
3.	COEFFICIENT OF COUPLING	K	.95 to .999
4.	RES-SECONDARY	R	.001 to 10000

STANDARD SINUSOIDAL VOLTAGE WAVEFORM MODEL



V = PO*SIN (2*P1*T*PI+P3) + P2 : IF P4 = 0

V = PO*EXP (-T/P4) * SIN (2*P1*T*PI+P3) + P2 : IF P4 < 0

PO = 1/2 amplitude (in volts)

P1 = frequency (in HZ)

P2 = average D.C. level (in volts)

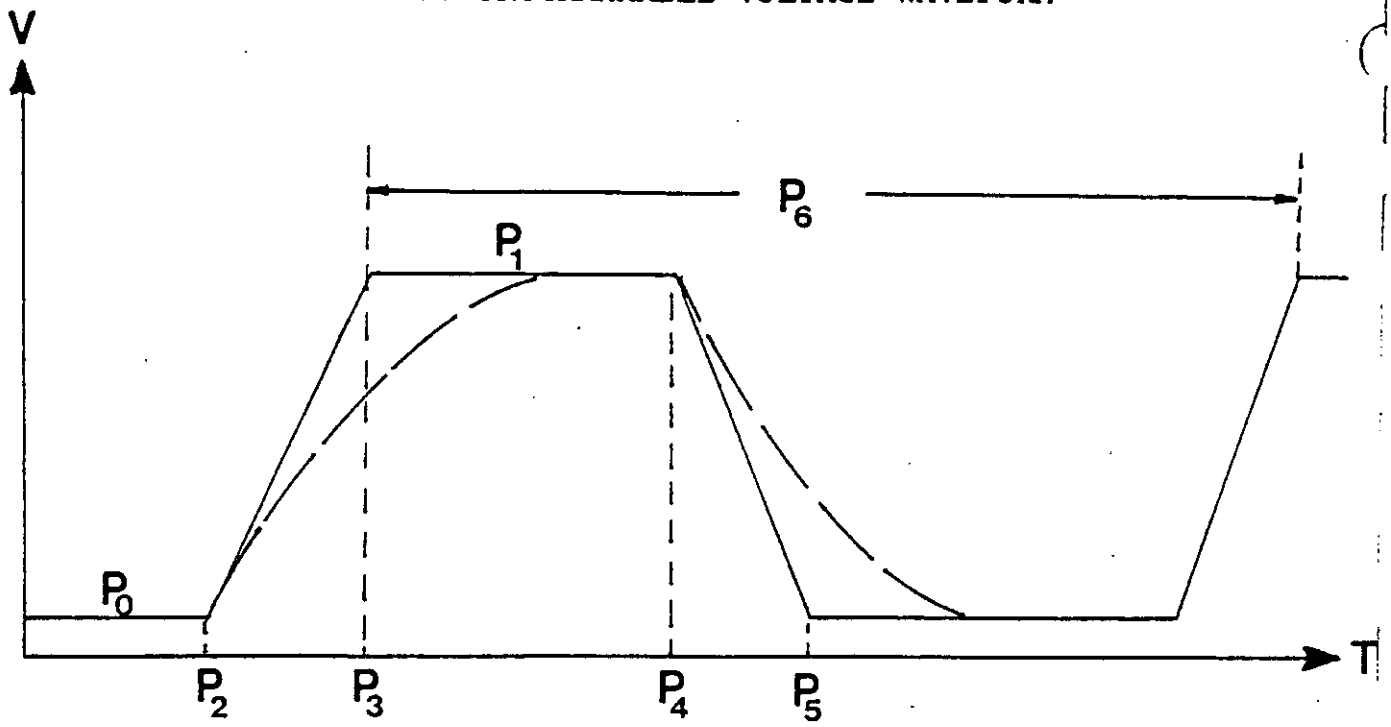
P3 = phase angle (in radians)

P4 = source resistance (in OHMS)

P5 = repetition period (in seconds used only if P6 is not zero)

P6 = exponential decay (in seconds. Set to zero if perfect sinusoid is desired).

STANDARD PROGRAMMABLE VOLTAGE WAVEFORM



1. Parameters 0 through 6 specified by the user.

2. Parameters 7 and 8 are calculated from the first 6 parameters.

3. Available as voltage sources only. For current source use in series with a resistor.

4. All time parameters (P2,P3,P4,P5) measured with respect to

   to T = 0 thus (P5>P4>P3>P2).

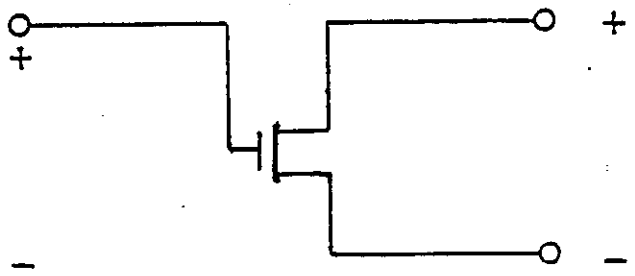
5. Rise and fall times must not be zero.

6. If P3<0 then the transition from level P0 to level P1 is an exponential of time constant P3 (instead of a ramp). Similarly if P5<0 the trailing edge ramp is replaced with an exponential transition of time constant P5.

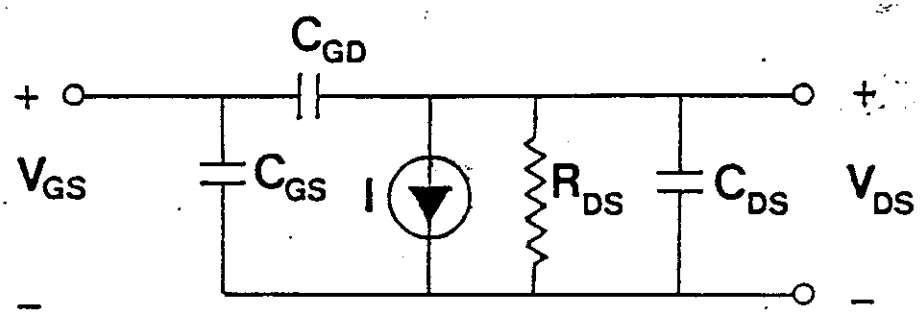
VII STANDARD COMPONENT MODELS

MOS TRANSISTOR MODEL FOR DC AND TRANSIENT ANALYSIS

SYMBOL:



MODEL:



EQUATIONS:

$$I=\begin{cases} 0 & : VGS-VT<=0 \\ B*(2*(VGS-VT)*VDS-VDS^{2}) & : VGS-VT>=VDS \\ B*(VGS-VT)*(VGS-VT) & : VGS-VT<VDS \end{cases}$$

$$VT=VTO+0.5*\sqrt{VSOURCE - VBODY}$$

MOS TRANSISTOR MODEL FOR DC AND TRANSIENT ANALYSIS

PARAMETERS:

	NAME	SYMBOL	TYPICAL VALUES
1.	BETA FACTOR (K'*W/L)	B	10^{-5} to 10^{-2}
2.	THRESHOLD VOLTAGE	VT	-5V to +5V
3.	GATE-DRAIN CAPACITANCE	CGD	.1pf to 100pf
4.	GATE-SOURCE CAPACITANCE	CGS	.1pf to 100pf
5.	DRAIN-SOURCE RESISTANCE	RDS	10K to 10M
6.	DRAIN-SOURCE CAPACITANCE	CDS	.1pf to 100pf
7.	LINEAR TRANSCONDUCTANCE(GM)	GM	10^{-5} to 10^{-2}

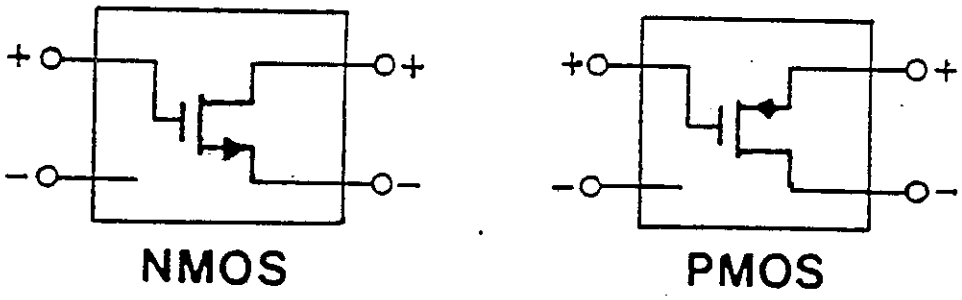
NOTES:

1. Polarity reversed for P Channel.
2. Body lead assumed connected to most negative circuit voltage for NMOS; most positive circuit voltage for PMOS.
3. Source/drain assignments are arbitrary for DC and Transient Analysis.
4. For enhancement mode NMOS use positive VT.
5. For enhancement mode PMOS use negative VT.
6. For depletion mode NMOS use negative VT.
7. For depletion mode PMOS use positive VT.

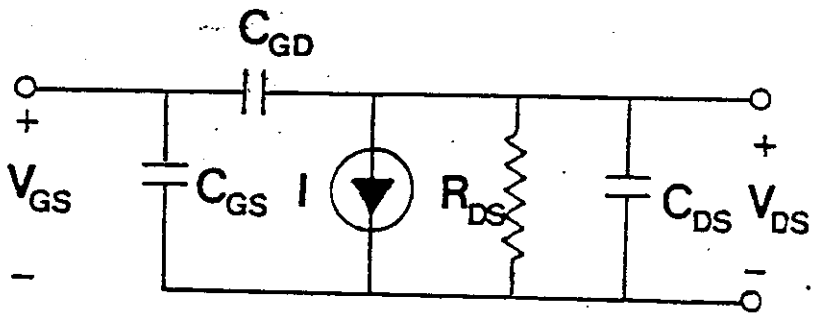
VII STANDARD COMPONENT MODELS

MOS TRANSISTOR MODEL FOR AC ANALYSIS

SYMBOL:



MODEL:



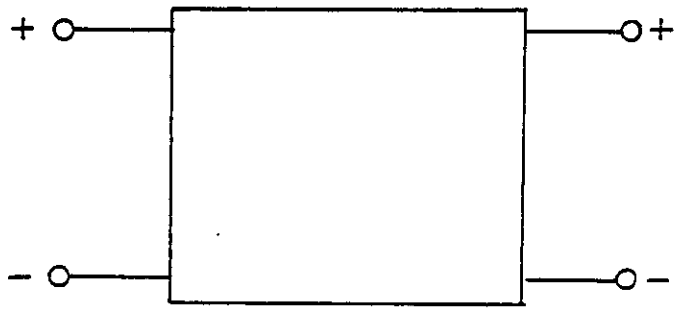
EQUATIONS: I=GM*VGS

NOTES: 1. Source and drain assignments are very important in AC analysis. Reversing them will produce equal gain of opposite polarity. In CMOS circuits this can be lead to cancellation of gain.

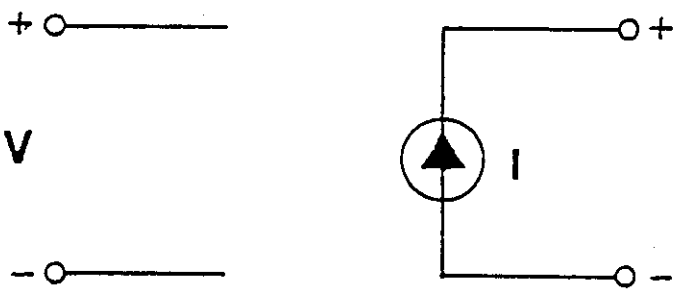
VII STANDARD COMPONENT MODELS

POLYNOMIAL SOURCE MODEL FOR ALL ANALYSIS MODES

SYMBOL:



MODEL:



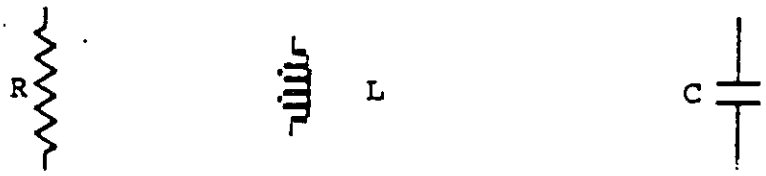
EQUATIONS: $I=A+B*V^{C}+D*V^{E}+F*V^{G}$

NOTES: 1. For AC ANALYSIS A, D, E, F, & G are set=0 and C is set=1 producing

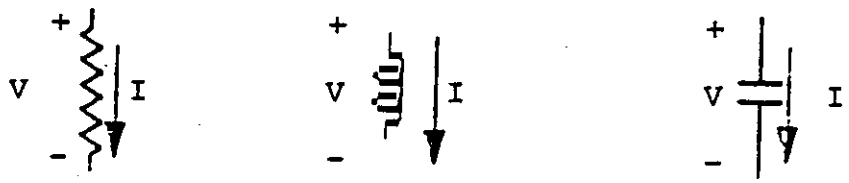
$$I=B*V$$

RESISTOR, INDUCTOR AND CAPACITOR MODELS

SYMBOL:



MODEL:



EQUATIONS:

$V=I*R$

$I=(1/L)\int V\,dt$

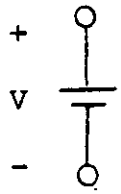
$V=L\,\frac{di}{dt}$

$I=C\,\frac{dv}{dt}$

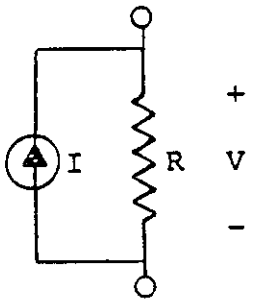
$I=(1/L)\int I\,dt$

BATTERY OR POWER SUPPLY

SYMBOL:



MODEL:

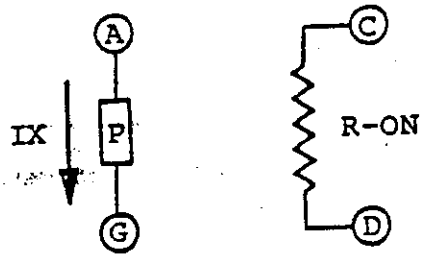


EQUATIONS: I= 1000*V
R= .001

SWITCH MODEL

SYMBOL:

MODEL:



PARAMETER FORMAT: SN1/N2/E

RULES OF OPERATION: Switch goes from off to on when

$$X \geq N1 * 10^{E}$$

Switch goes from on to off when

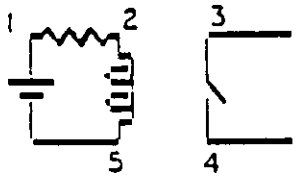
$$X \leq N2 * 10^{E}$$

Where

$$X = \begin{cases} VA - VB & \text{if } S=V \\ IX & \text{if } S=I \text{ and } P \text{ is an inductor} \\ Time & \text{if } S=T \end{cases}$$

EXAMPLES

Each of the following examples will refer to this network.



EXAMPLE 1: TIME DEPENDENT SWITCH

	-	+	-	+	PARAMETER
SWITCH	0	0	4	3	T1/2/-3

This line in a netlist would create a switch that connects nodes 4 and 3 when:

$$1*10^{-3} \leq T \leq 2*10^{-3} \quad \text{(T=time in seconds)}$$

During this time the resistance of the switch would be R-ON (specified for all switches during the Transient Analysis Prologue). During all other times (before and after the above interval) the switch resistance would be infinite.

EXAMPLE 2: VOLTAGE DEPENDENT SWITCH

	-	+	-	+	PARAMETER
SWITCH	5	2	4	3	V1/2/0

This line in a netlist would create a switch that connects nodes 4 and 3 when:

$$1*10^{0} \leq V2 - V5 \leq 2*10^{0}$$

OR

$$1 \leq V2 - V5 \leq 2$$

Whenever the differential voltage V2-V5 is between 1 and 2 volts the switch connects nodes 4 and 3 through a resistance of R-ON (specified during the Transient Analysis Prologue). For all other values of V2-V5 the switch is open (eg. its impedence is infinite).

NOTE: This type of switch can only be added to a network (or netlist) through the Analyzer's Network Editor. The Designer Module can only manipulate time-dependent switches.

EXAMPLE 3: CURRENT-DEPENDENT SWITCH

	-	+	-	+	PARAMETER
SWITCH	5	2	4	3	I1/2/-6

This line in a netlist would create a switch that connects nodes 4 and 3 when:

$$1*10^{-6} < IX < 2*10^{-6}$$

Whenever the current flowing through the inductor is between 1 and 2 micro-amps the switch connects nodes 4 and 3 through a resistance of R-ON (specified during the Transient Analysis Prologue). For all other values of IX the switch impedance is infinite (eg. it is open)

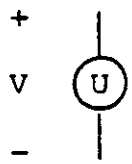
NOTE:
1. This type of switch may be used only if the component P is an inductor.
2. This type of switch can only be added to a network (or netlist) through the Analyzer's Network Editor. The Designer Module can only manipulate time-dependent switches.

GENERAL NOTES

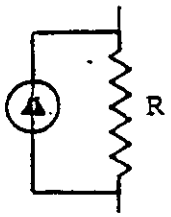
1. Switches are available only for Transient Analysis. They are ignored in DC and AC analysis modes.
2. Normally the parameter N1 is greater than N2. If the parameter N1 is less than N2, the switch operation is complimented; off when it normally is on and vice versa.

USER SOURCE

SYMBOL:



MODEL:



EQUATIONS: R=.001

I= V/R= 1000•V

V= User specified time-dependent voltage

APPENDIX A

MAXIMUM SPECIFICATIONS

SPECIFICATION	MAXIMUM VALUE
NODES: TRANSIENT & DC ANALYSIS	40
NODES: AC ANALYSIS	23 (25 IBM)
STANDARD LIBRARY COMPONENTS	5
BATTERIES	10
RESISTORS	60
CAPACITORS	60
INDUCTORS	40
DIODES	20
VSIN SOURCE	5
V(T) SOURCE	5
BIPOLAR TRANSISTORS	20
MOS DEVICES	20
TRANSFORMERS	10
OPAMPS	20
SWITCHES	10
USER SOURCES	1
POLYNOMIAL SOURCES	10

APPENDIX B

HARDWARE REQUIREMENTS

A. APPLE II SYSTEM

1. APPLE II with Applesoft in ROM on the mother board or APPLE II PLUS or APPLE II-e
2. 64K RAM (Standard 48K RAM + 16K RAM card or 16K Language card)
3. Two Disk Drives (DOS 3.3)
4. Optional printer

B. IBM PC SYSTEM

1. IBM PC with Color Graphics Adapter Board.
2. 128K RAM
3. Two Disk Drives (single or double-sided DOS 1.1)
4. Optional printer

APPENDIX C

THINGS TO WATCH OUT FOR

1. Isolated nodes: All of the analysis routines use matrix inversion to solve a system of circuit equations. If you leave out a circuit node (in the node numbering process) the inversion routines will encounter division by zero. The Analyzer checks for missing nodes and will not allow you to run an analysis if your networks contains missing nodes.

   However, a node can be "essentially" missing if the smallest impedance from that node to other nodes in the circuit is "too large". By "too large" is meant that the impedance is generally greater than 1E08. This commonly occurs only with diodes, whose true reversed biased impedance exceeds 1E08. We could cause it to occur by adding a 2-resistor divider network to the BRC circuit and setting each resistor to 1E09. The extra node formed by the junction of the divider would be "essentially isolated" since the computers' precision is less than the impedance and it is essentially set to infinity, causing isolation.

APPENDIX C

THINGS TO WATCH OUT FOR

2. Time increments:

When a Transient Analysis is run the user must select a DELTA T or time increment. If the circuit contains some fast and some slow sections the DELTA T must be chosen to be smaller than the shortest (or fastest) time constant. For example, if in the BRC circuit we added a resistor of value 1 ohm from node 2 to a new node (#3) and from that node a capacitor to ground of value 100pf, the circuit would now have two time constants:

1) 100ns (the old one)
2) 0.1ns (the new one)

Simulating this circuit would require specifying a DELTA T of no more than 0.1ns and preferably smaller.

If you select a DELTA T that is too large the waveforms displayed may exhibit erratic oscillation and the results will be less than accurate.

Generally this effect occurs only with networks using the non-linear components, MOS devices and Polynomial sources.

3. Switches:

Care should be taken when using switches. It is tempting to set the switch impedance to some very low value. This may cause roundoff problems due to the limited precision available on the computer. As a general rule never connect widely different impedances to a common node. Widely different means that the ratio of any one impedance to any other on the same node should not exceed 1E06.

APPENDIX E

EXAMPLES

This section contains ten examples of various circuits ranging from the simple BRC network to power supply and active filter circuits. Several of these circuits are contained on the data diskette and can be recalled from either the Analyzer or or Designer menu by using the following file names.

EXAMPLE

BRC

PRLC

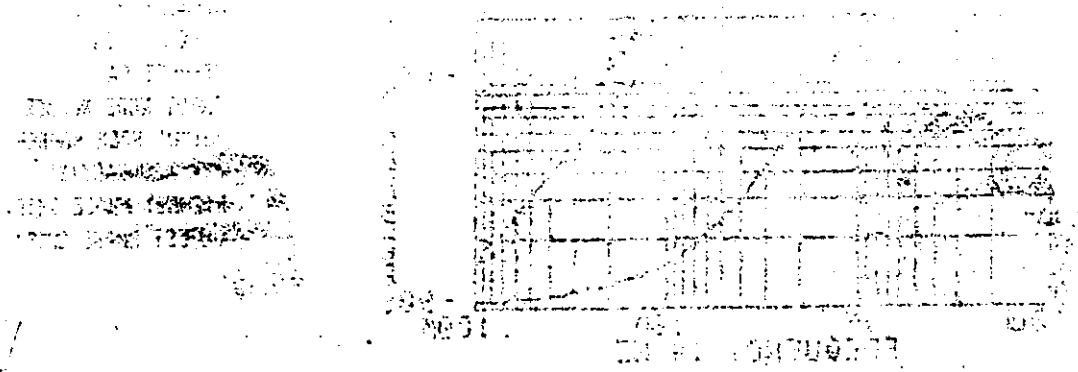
MOS INVERTER-R

MOS OSCILLATOR

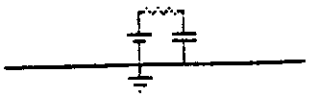
LINEAR AMPLIFIER

REGULATED POWER SUPPLY

CHESBYSHEF 6TH ORDER FILTER

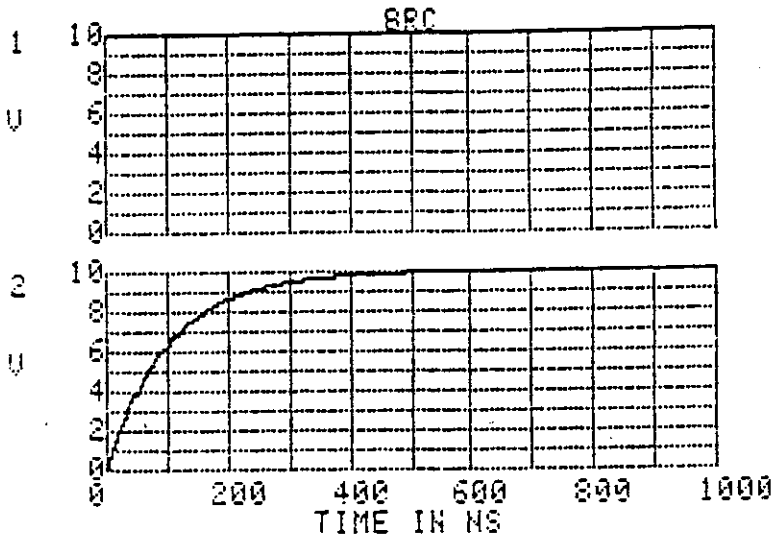


APPENDIX E
EXAMPLES



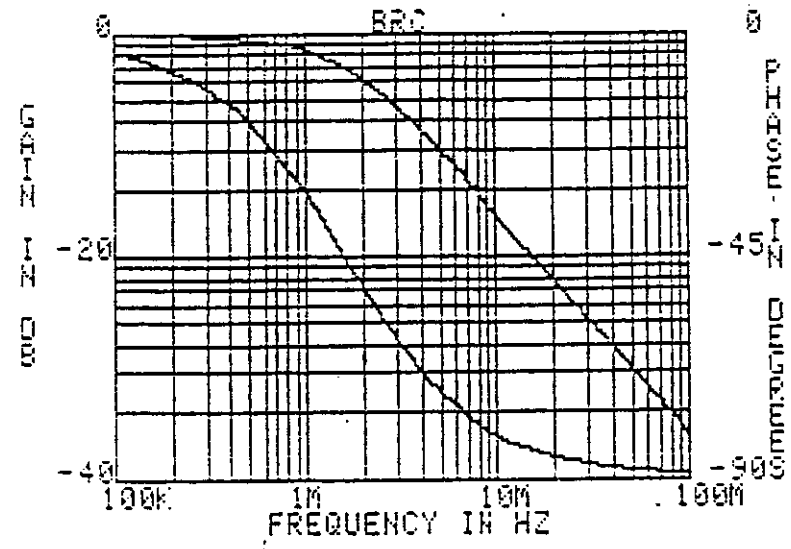
NETLIST
SRC CIRCUIT

REF	COMPONENT	CONNECTIONS				PARAMETER
		IN		OUT		OR
NO.	NAME	-	+	-	+	TYPE
1:	BATTERY	0	1	0	0	10
2:	RESISTOR	1	2	0	0	1E3
3:	CAPACITOR	2	0	0	0	1E-10



ANALYSIS LIMITS

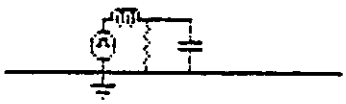
MAXIMUM SIM TIME(SEC)	1E-06
MAXIMUM DELTA TIME(SEC)	5E-09
MINIMUM ACCURACY (%)	5
UPPER TRACE NODE(S)	1
OFFSET FOR #1	0
SCALE FACTOR FOR #1	1
LOWER TRACE NODE(S)	2
OFFSET FOR #2	0
SCALE FACTOR FOR #2	1



ANALYSIS LIMITS

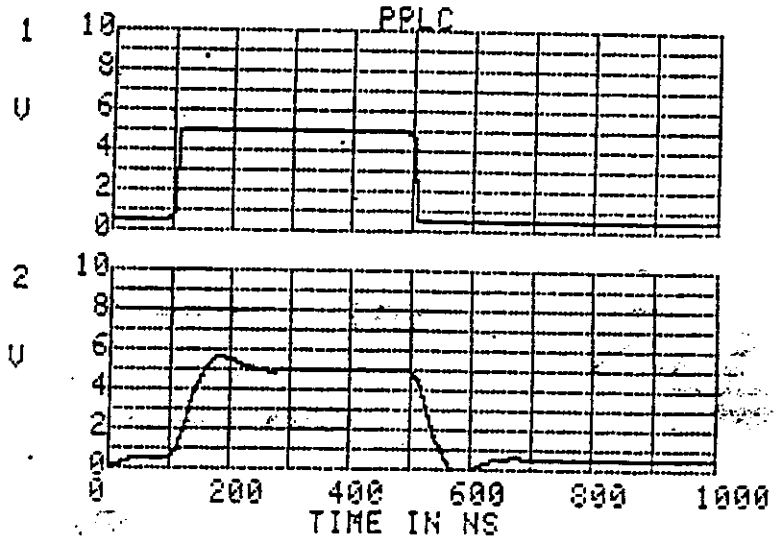
LOWEST FREQUENCY	100000
HIGHEST FREQUENCY	100000000
LOWEST GAIN	.01
HIGHEST GAIN	1
INPUT NODE NUMBER	1
OUTPUT NODE NUMBER	2
MIN ACCURACY(%)	2
HIGHEST PHASE SHIFT	0
LOWEST PHASE SHIFT	-90

APPENDIX E
EXAMPLES



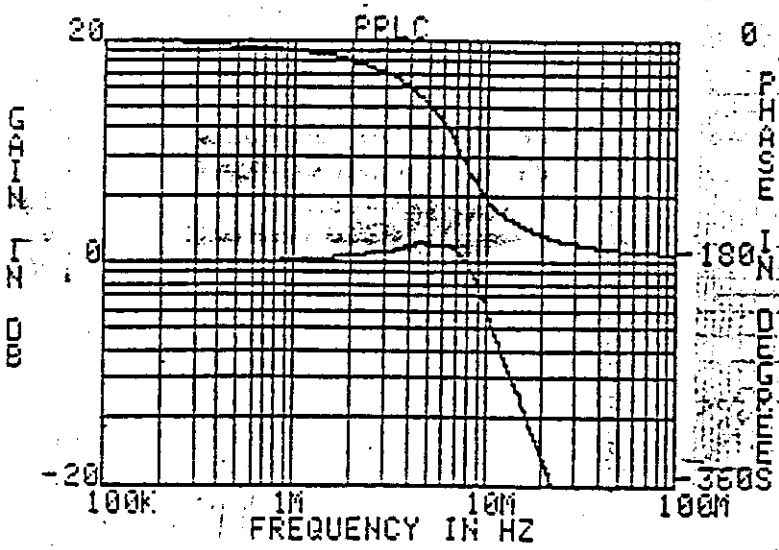
NETLIST
PRLC CIRCUIT

REF	COMPONENT	CONNECTIONS IN		OUT		PARAMETER OR	
NO.	NAME	-	+	-	+	TYPE	
1:	V(T)	0	1	0	0	3	P0=.5 P1=5 P2=1E-07 P3=1.1E-07 P4=5E-07 P5=5.1E-07 P6=1E-06
2:	INDUCTOR	1	2	0	0	1E-6	
3:	RESISTOR	2	0	0	0	50	
4:	CAPACITOR	2	0	0	0	5E-10	



ANALYSIS LIMITS

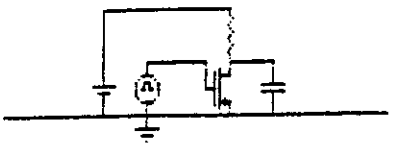
MAXIMUM SIM TIME(SEC)	1E-06
MAXIMUM DELTA TIME(SEC)	5E-09
MINIMUM ACCURACY (Z)	5
UPPER TRACE NODE(S)	1
OFFSET FOR #1	0
SCALE FACTOR FOR #1	1
LOWER TRACE NODE(S)	2
OFFSET FOR #2	0
SCALE FACTOR FOR #2	1



ANALYSIS LIMITS

LOWEST FREQUENCY	100000
HIGHEST FREQUENCY	100000000
LOWEST GAIN	.1
HIGHEST GAIN	10
INPUT NODE NUMBER	1
OUTPUT NODE NUMBER	2
MIN ACCURACY(Z)	2
HIGHEST PHASE SHIFT	0
LOWEST PHASE SHIFT	-360

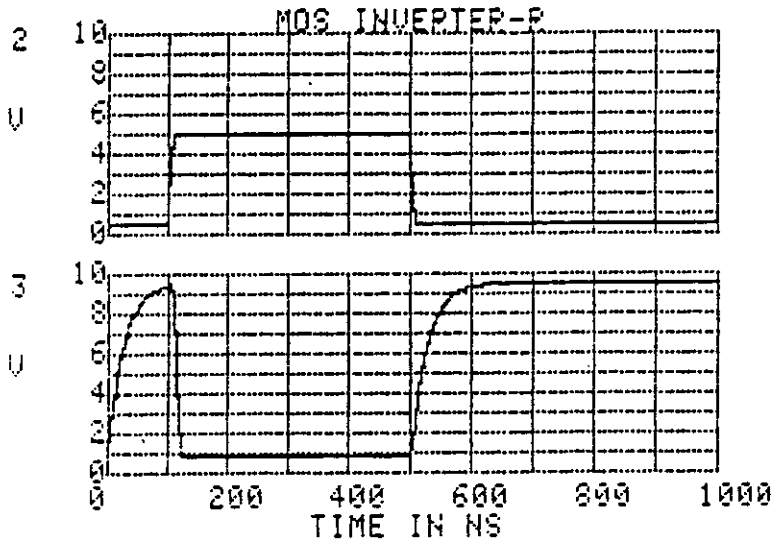
APPENDIX E
EXAMPLES



NETLIST

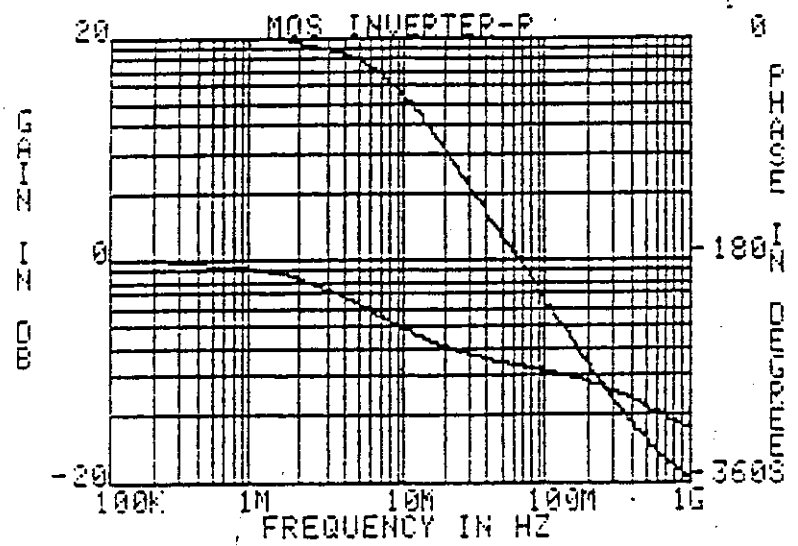
MOS INVERTER-R CIRCUIT

REF	COMPONENT	CONNECTIONS				PARAMETER
		IN		OUT		OR
NO.	NAME	-	+	-	+	TYPE
1:	BATTERY	0	1	0	0	9.5
2:	V(T)	0	2	0	0	3 P0=.5 P1=5 P2=1E-07 P3=1.1E-07 P4=5E-07 P5=5.1E-07 P6=1E-06
3:	NMOS TRANS.	0	2	0	3	0 B=.01 VT=2 CGD=1E-11 CGS=1E-11 RDS=1000000 CDS=1E-11 GM=.0
4:	CAPACITOR	3	0	0	0	1E-10
5:	RESISTOR	1	3			200



ANALYSIS LIMITS

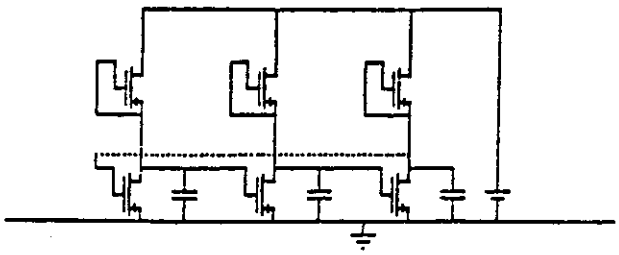
MAXIMUM SIM TIME(SEC)	1E-06
MAXIMUM DELTA TIME(SEC)	2E-9
MINIMUM ACCURACY (Z)	5
UPPER TRACE NODE(S)	2
OFFSET FOR #1	0
SCALE FACTOR FOR #1	1
LOWER TRACE NODE(S)	3
OFFSET FOR #2	0
SCALE FACTOR FOR #2	1



ANALYSIS LIMITS

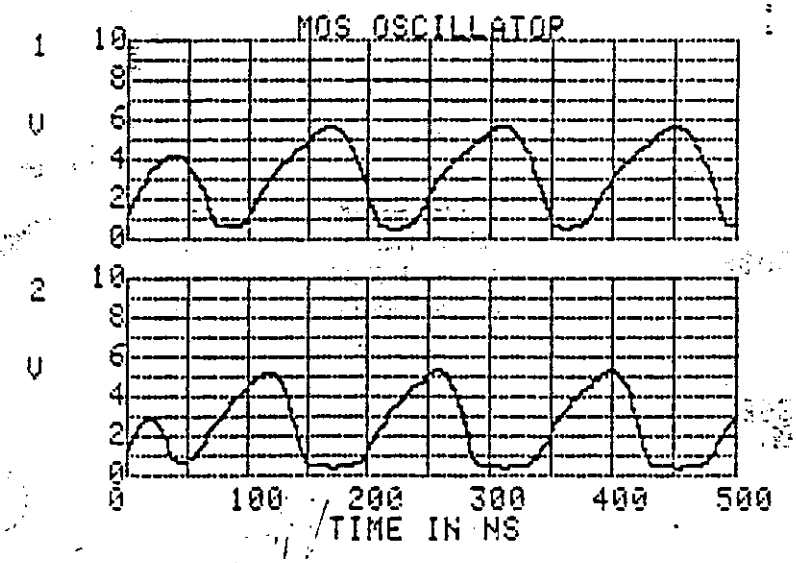
LOWEST FREQUENCY	100000
HIGHEST FREQUENCY	1E+09
LOWEST GAIN	.1
HIGHEST GAIN	10
INPUT NODE NUMBER	2
OUTPUT NODE NUMBER	3
MIN ACCURACY(Z)	2
HIGHEST PHASE SHIFT	0
LOWEST PHASE SHIFT	-360

APPENDIX E
EXAMPLES



NETLIST
MOS OSCILLATOR CIRCUIT

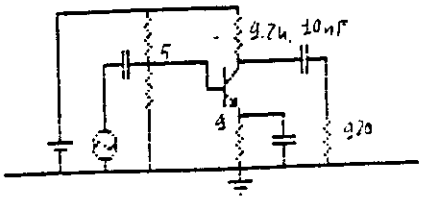
REF	COMPONENT	CONNECTIONS				PARAMETER
		IN		OUT		OR
NO.	NAME	-	+	-	+	TYPE
1:	NMOS TRANS.	0	1	0	2	0 B=.01 VT=2 CGD=1E-11 CGS=1E-11 RDS=1000000 CDS=1E-11 GM=.05
2:	NMOS TRANS.	0	2	0	3	B=.01 VT=2 CGD=1E-11 CGS=1E-11 RDS=1000000 CDS=1E-11 GM=.05
3:	NMOS TRANS.	0	3	0	1	B=.01 VT=2 CGD=1E-11 CGS=1E-11 RDS=1000000 CDS=1E-11 GM=.05
4:	CAPACITOR	1	0	0	0	1E-10
5:	CAPACITOR	2	0	0	0	1E-10
6:	BATTERY	0	4	0	0	10
7:	NMOS TRANS.	0	1	1	4	1 B=.01 VT=-2 CGD=1E-11 CGS=1E-11 RDS=1000000 CDS=1E-12 GM=.05
8:	NMOS TRANS.	0	3	3	4	1 B=.01 VT=-2 CGD=1E-11 CGS=1E-11 RDS=1000000 CDS=1E-12 GM=.05
9:	NMOS TRANS.	0	2	2	4	1 B=.01 VT=-2 CGD=1E-11 CGS=1E-11 RDS=1000000 CDS=1E-12 GM=.05
10:	CAPACITOR	3	0	2	4	2E-10



ANALYSIS LIMITS

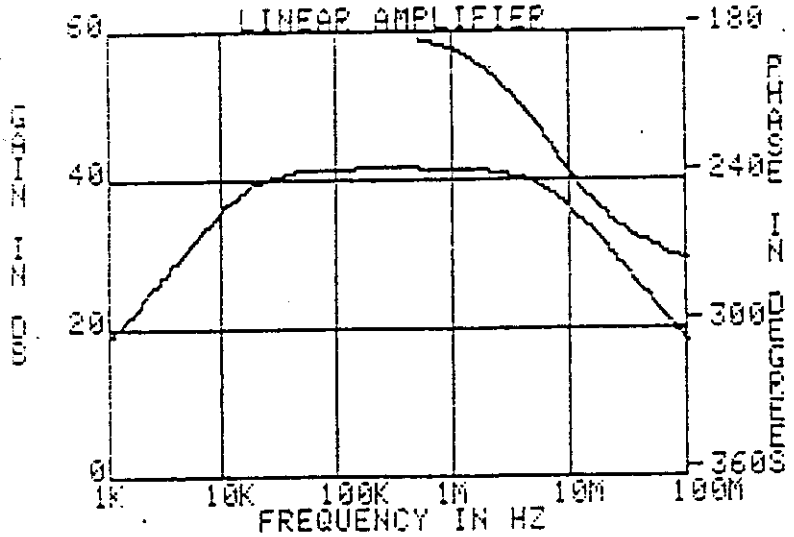
MAXIMUM SIM TIME(SEC)	5E-7
MAXIMUM DELTA TIME(SEC)	2E-9
MINIMUM ACCURACY (%)	5
UPPER TRACE NODE(S)	1
OFFSET FOR #1	0
SCALE FACTOR FOR #1	1
LOWER TRACE NODE(S)	2
OFFSET FOR #2	0
SCALE FACTOR FOR #2	1

APPENDIX E
EXAMPLES



NETLIST
LINEAR AMPLIFIER CIRCUIT

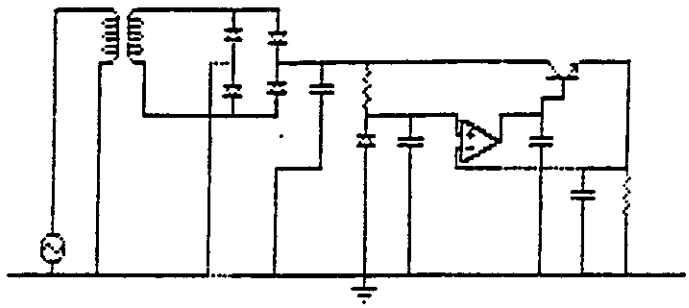
REF NO.	COMPONENT NAME	CONNECTIONS IN -	IN +	OUT -	OUT +	PARAMETER OR TYPE	
1:	VSIN	0	2	0	0	2	
2:	CAPACITOR	2	5	0	0	1E-6	
3:	RESISTOR	5	1	0	0	1E5	
4:	RESISTOR	5	0	0	0	1E4	
5:	RESISTOR	6	1	0	0	4700	
6:	BATTERY	0	1	0	0	10	
7:	RESISTOR	3	0	0	0	470	
8:	CAPACITOR	3	0	0	0	5E-7	
9:	CAPACITOR	6	4	0	0	1E-6	
10:	RESISTOR	4	0	0	0	4700	
11:	NPN TRANS.	4	5	3	6	2	B=50 D$=2 FT=50000000 ICF=3E-03 RSAT=5 CBE=3.672E-10 CBC=1E-11



ANALYSIS LIMITS

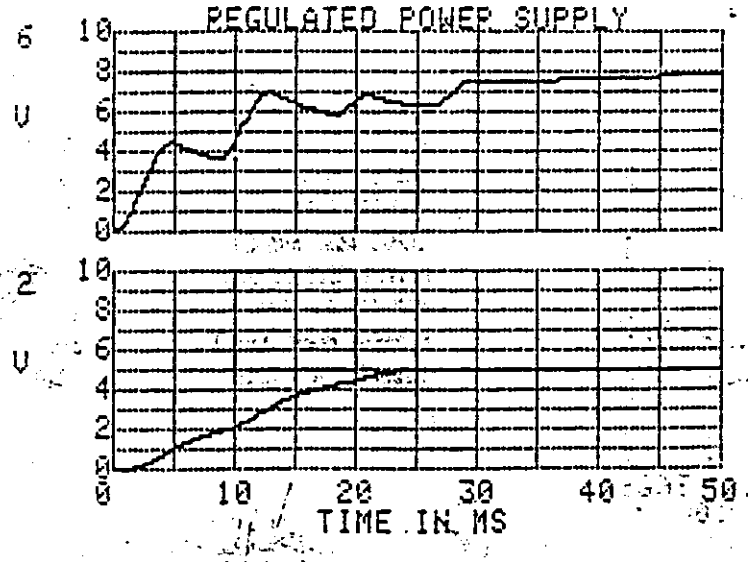
LOWEST FREQUENCY	1000
HIGHEST FREQUENCY	100000000
LOWEST GAIN	1
HIGHEST GAIN	1000
INPUT NODE NUMBER	2
OUTPUT NODE NUMBER	6
MIN ACCURACY(%)	2
HIGHEST PHASE SHIFT	-180
LOWEST PHASE SHIFT	-350

APPENDIX E
EXAMPLES



NETLIST
REGULATED POWER SUPPLY CIRCUIT

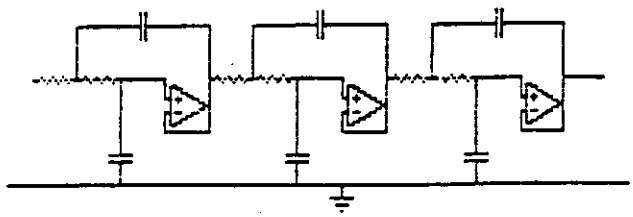
REF	COMPONENT	CONNECTIONS IN		OUT		PARAMETER OR	
NO.	NAME	-	+	-	+	TYPE	
1:	VSIN	0	1	0	0	0	
2:	TRANSFORMER	0	1	3	7	0	LP=.01 N=6 K=.99 R=1E-03 =0 =0 =0
3:	RESISTOR	6	4	0	0	1000	
4:	DIODE	4	0	0	0	3	IO=1E-13 VZ=5 RZ=10 RF=10 VT=.026 RP=10000 =0
5:	OPAMP	2	4	0	5	0	RI=1000000 AO=1000 RO=100 VOFF=1E-04 VMAX=30 CO=5E-08 =0
6:	NPN TRANS.	0	5	2	6	0	B=66 BR=0 FT=125000000 ICF=2E-03 RSAT=5 CBE=9.794E-11 CBC=1E-12
7:	DIODE	3	0	0	0	1	IO=1E-12 VZ=200 RZ=20 RF=1 VT=.026 RP=10000 =0
8:	DIODE	7	0	0	0	1	IO=1E-12 VZ=200 RZ=20 RF=1 VT=.026 RP=10000 =0
9:	DIODE	6	7	0	0	1	IO=1E-12 VZ=200 RZ=20 RF=1 VT=.026 RP=10000 =0
10:	DIODE	6	3	0	0	1	IO=1E-12 VZ=200 RZ=20 RF=1 VT=.026 RP=10000 =0
11:	RESISTOR	2	0	0	0	1000	
12:	CAPACITOR	4	0	0	0	1E-5	
13:	CAPACITOR	6	0	0	0	1E-3	
14:	CAPACITOR	5	0	0	0	1E-5	
15:	CAPACITOR	2	0	0	0	1E-3	



ANALYSIS LIMITS

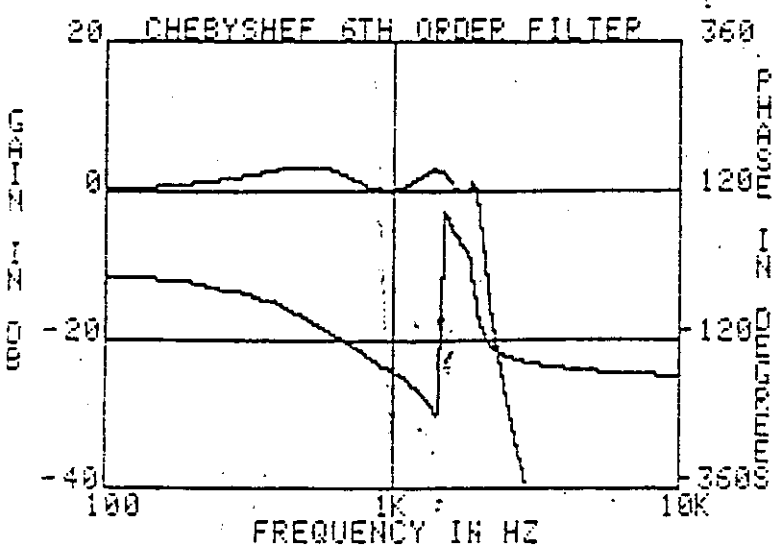
MAXIMUM SIM TIME(SEC)	50E-3
MAXIMUM DELTA TIME(SEC)	2E-4
MINIMUM ACCURACY (%)	2
UPPER TRACE NODE(S)	6
OFFSET FOR #1	0
SCALE FACTOR FOR #1	1
LOWER TRACE NODE(S)	2
OFFSET FOR #2	0
SCALE FACTOR FOR #2	1

APPENDIX E
EXAMPLES



NETLIST
CHEBYSHEF 6TH ORDER FILTER CIRCUIT

REF NO.	COMPONENT NAME	CONNECTIONS IN -	IN +	OUT -	OUT +	PARAMETER OR TYPE
1:	RESISTOR	7	8	0	0	28422
2:	RESISTOR	8	1	0	0	77782
3:	OPAMP	2	1	0	2	1 RI=1000000 AO=1000 RO=100 VOFF=1E-04 VMAX=30 CO=5E-08 =0
4:	CAPACITOR	1	0	0	0	60E-12
5:	CAPACITOR	2	8	0	0	5E-8
6:	RESISTOR	2	9	0	0	12613
7:	RESISTOR	9	3	0	0	19243
8:	OPAMP	4	3	0	4	1 RI=1000000 AO=1000 RO=100 VOFF=1E-04 VMAX=30 CO=5E-08 =0
9:	CAPACITOR	3	0	0	0	1E-9
10:	CAPACITOR	4	9	0	0	5E-8
11:	RESISTOR	4	10	0	0	8220
12:	RESISTOR	10	5	0	0	17350
13:	CAPACITOR	5	0	0	0	1E-8
14:	OPAMP	6	5	0	6	1 RI=1000000 AO=1000 RO=100 VOFF=1E-04 VMAX=30 CO=5E-08 =0
15:	CAPACITOR	6	10	0	0	5E-8



ANALYSIS LIMITS

LOWEST FREQUENCY	100
HIGHEST FREQUENCY	10000
LOWEST GAIN	.01
HIGHEST GAIN	10
INPUT NODE NUMBER	7
OUTPUT NODE NUMBER	6
MIN ACCURACY(%)	1
HIGHEST PHASE SHIFT	360
LOWEST PHASE SHIFT	-360

MICRO-CAP

MICROCOMPUTER CIRCUIT ANALYSIS PROGRAM

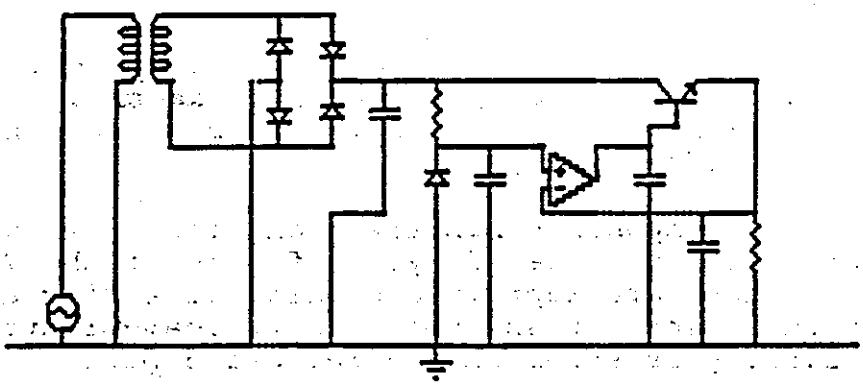
MICRO-CAP is a professional design tool, created to enhance the productivity of electronics design by providing an interactive drawing and analysis system. It allows the engineer to quickly design and predict the performance of a circuit without having to actually build it.

The software product enables the user to:

- Draw an electronic circuit diagram directly on the CRT screen.
- Perform an A/C (Bode) analysis showing Gain and Phase Shift vs. frequency.
- Run a time-domain simulation of the circuit responding to user-defined input sources.
- Perform a D/C Transfer characteristic analysis showing output voltages vs input voltage.

It's like building a breadboard and hooking up signal sources and instruments to see what happens...except that it's faster.

Circuit diagrams are drawn directly on the screen using the Designer Module. Using the keyboard you move the drawing cursor around on the screen adding or deleting components. Each time you add a component the system draws it at the cursor position. Drawing interconnecting lines allows you to create any type of circuit diagram. Completed circuit diagrams are then saved in a diskette file. A typical completed circuit diagram looks like this:



When the drawing is complete the Analysis program prepares the equations needed for the simulation. That program creates (and allows you to edit if you wish) the Network listing. A typical Network listing looks like this:

NETLIST
REGULATED POWER SUPPLY CIRCUIT

REF	COMPONENT	CONNECTIONS				PARAMETER
		IN		OUT		OR
NO.	NAME	-	+	-	+	TYPE
1:	TRANSFORMER	0	1	3	7	0
2:	DIODE	7	0	0	0	0
3:	DIODE	6	7	0	0	0
4:	DIODE	6	3	0	0	0
5:	DIODE	3	0	0	0	0
6:	RESISTOR	6	4	0	0	1000
7:	DIODE	4	0	0	0	3
8:	OPAMP	2	4	0	5	0
9:	NPN TRANS.	0	5	2	6	0
10:	RESISTOR	2	0	0	0	100
11:	CAPACITOR	2	0	0	0	1E-4
12:	VSIN	0	1	0	0	0

Components are specified in a network in one of two ways:

A) By their parametric value-Resistors, Inductors, Capacitors, Batteries.

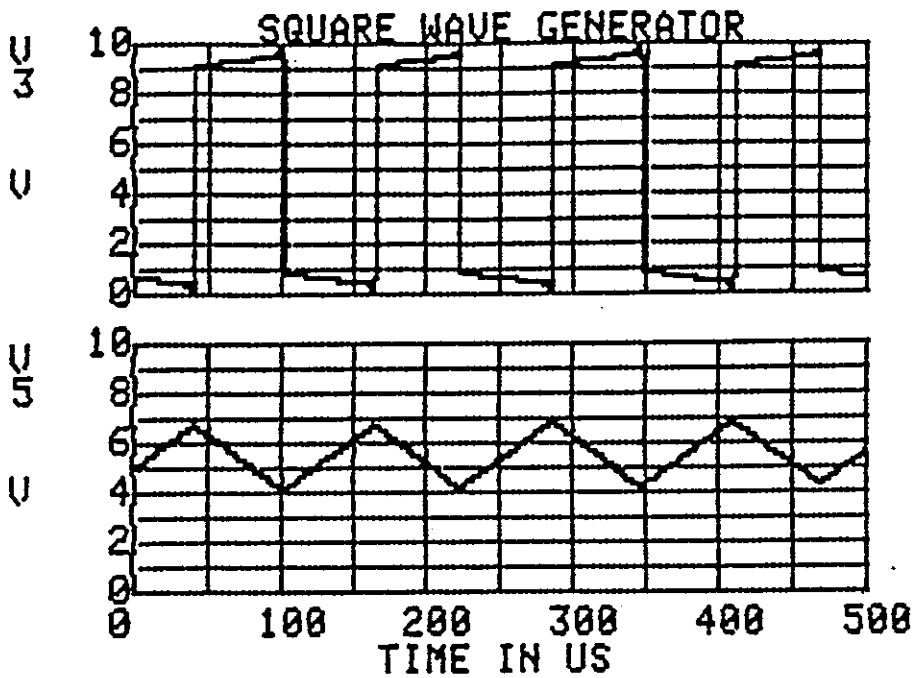
B) By their type number - all other components.

Category B Components are called STANDARD COMPONENTS.

You can define and use in any given network up to 5 different types of each Standard Component. For example, you may use more than 5 OP AMPS in a given network, but you can only use a maximum of 5 different types.

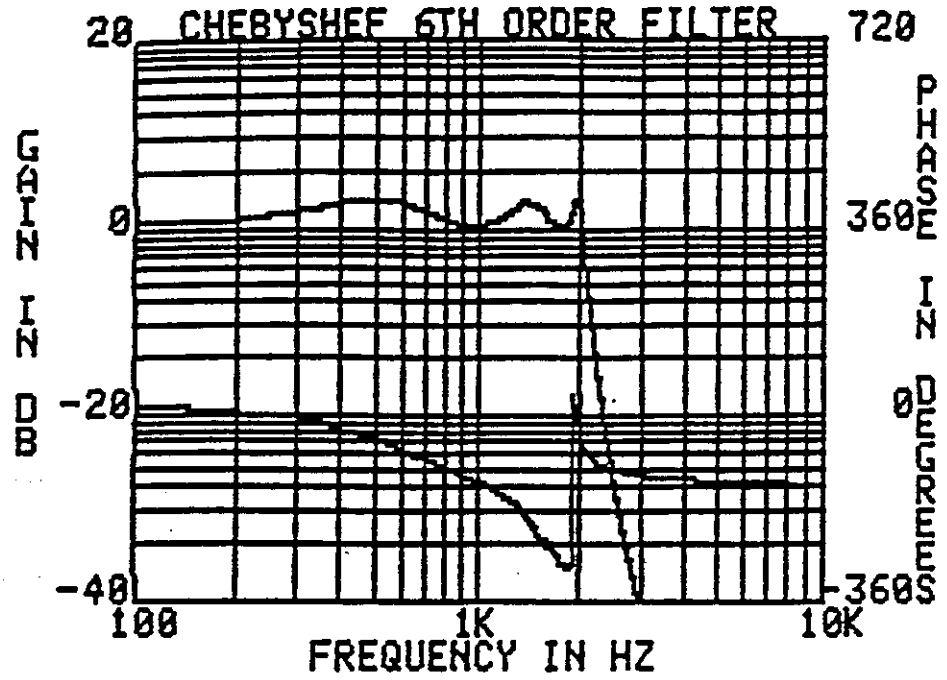
The Standard Components Library contains the parametric values for each of the 5 types of each of the 7 Standard Components. These are kept in a special disk file and can be edited by the user at any time. A typical printout of the Standards Library is shown on the following page.

Following the creation of a circuit you can perform a Transient Analysis. In this mode the system calculates the voltage as a function of time on any two nodes in the circuit. The results look a lot like a dual-trace oscilloscope display:

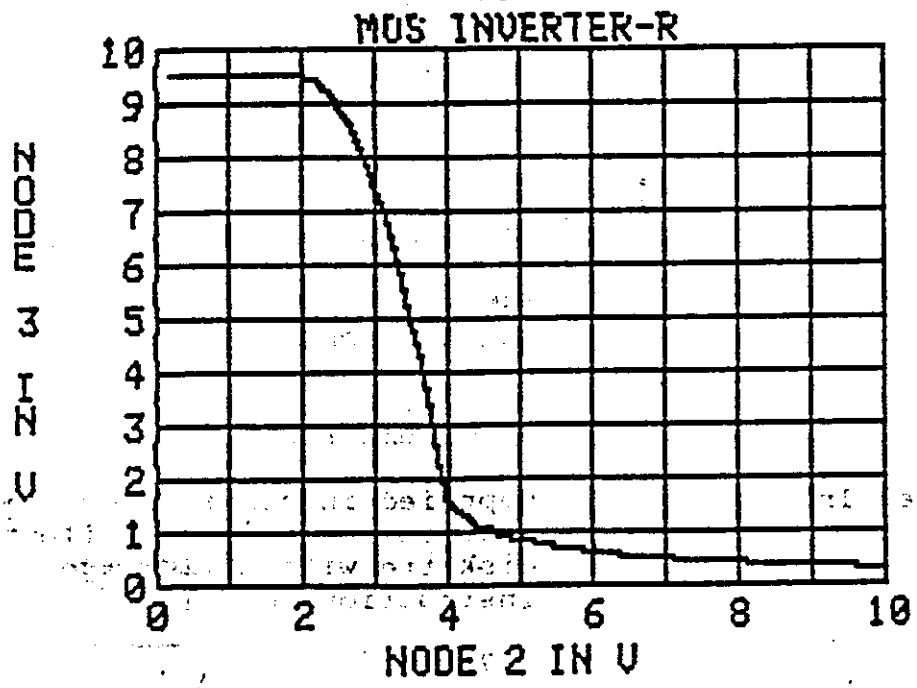


Transient Analysis can also be generated in printer plot or tabular fashion.

Alternatively you can perform an AC analysis.



or a D.C. analysis.



MICRO-CAP
AT A GLANCE

Analysis Modes	AC Analysis (Bode Plots). DC Transfer Characteristic. Non-Linear Time Domain.
Input	Drawn Circuit Diagram. Keyed Circuit Description. Standard Components Library.
Output	CRT Bode Analysis (or Graphics dump). CRT DC Analysis (or Graphics dump). CRT Circuit Diagram (or Graphics dump to Printer). CRT Waveforms (or Graphics dump to Printer). Printer Plot of Waveforms. Printer Tabular Listing of Node Voltages. Standards Library. Network Listing.
Components Supported	Resistors, Inductors, Capacitors, Batteries, Sinusoidal Voltage Sources, Programmable Waveform Voltage Sources, Diodes, OP AMPS, Bipolar Transistors (NPN & PNP) MOS Transistors (PMOS & NMOS), Transformers.
Maximum # of Nodes	40 (23 AC)
Hardware Required	APPLE II with Applesoft in ROM, or APPLE II Plus or APPLE IIe with 64K RAM. DOS 3.3, 2 DRIVES 80 Column Printer (Optional). IBM PC, 128K RAM. Color Graphics Adapter Board. 2 Disk Drives DOS 1.1 80 Column Printer (Optional).
Medium Supplied In.	Supplied in compiled object code on a 5-1/4" mini floppy diskette with a 120 page instruction manual.
Product Price	$475.00
Manual and Demo Disk Package	$30.00 (Refundable towards product purchase).

LOGIC SIMULATOR AND DESIGNER

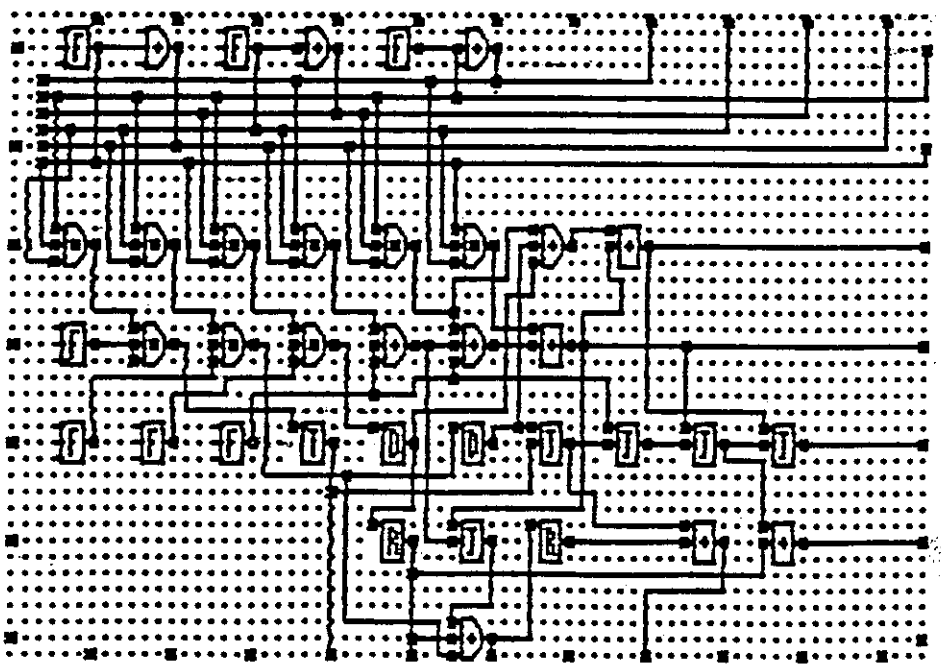
A professional design tool, this product was created to enhance the productivity of electronics design by providing an interactive drawing and simulation system, allowing the engineer to quickly design and predict the performance of a circuit without having to actually build it.

This software product enables the user to:

- Draw a logic diagram directly on the CRT screen.
- Run a state simulation of the networks responding to user-defined input sources.

It's like building a breadboard and hooking up signal sources and logic analyzers to see what happens...except that it's faster.

Logic diagrams are drawn directly on the screen using the Designer program. Using the keyboard commands you move the drawing cursor around on the screen adding or deleting gates. Each time you add a gate the system draws it at the cursor position. Drawing interconnecting lines and contacting gate input and output nodes using the PLOT and CONTACT commands allows you to create any type of logic network. Completed logic diagrams are then saved in a diskette file. A typical completed diagram looks like this:



When the drawing is complete the INPUT program prepares the database needed for the simulation. That program creates (and allows you to edit if you wish) the Network listing. A typical Network listing looks like this:

NODE	TYPE	A	B	C
1	SOURCE..A = SOURCE #	0	0	0
2	SOURCE..A = SOURCE #	1	0	0
3	SOURCE..A = SOURCE #	2	0	0
4	NOR.....OUT=NOT(A+B+C)	1	2	3
5	NAND....OUT=NOT(A+B+C)	3	2	0
6	D FLOP..INPUT=A	2	0	0
7	T FLOP..INPUT=A	3	0	0
8	JKFLOP..A=J B=K	2	5	0
9	S/R.....A=IN B=LENGTH	4	7	0
10	D FLOP..INPUT=A	7	0	0
11	NOR.....OUT=NOT(A+B+C)	3	6	9
12	EX-OR...NOTA*B+A*NOTB	2	7	0
13	EX-OR...NOTA*B+A*NOTB	1	8	0
14	EX-OR...NOTA*B+A*NOTB	12	13	0
15	NAND....OUT=NOT(A*B*C)	2	13	12
16	JKFLOP..A=J B=K	9	3	0
17	NOR.....OUT=NOT(A+B+C)	1	3	0
18	NOR.....OUT=NOT(A+B+C)	1	4	5
19	NAND....OUT=NOT(A*B*C)	13	18	16
20	NAND....OUT=NOT(A*B*C)	5	11	19

User's may create their own MACROS using the MACRO editor. Up to 16 different 3-input combinational functions can be defined and subsequently used in any Network. A typical MACRO Worksheet looks like this:

MACRO TRUTH TABLE EDITOR

INPUT STATES	MACRO NUMBER															
											1	1	1	1	1	1
A B C	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5
0 0 0	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0
0 0 1	0	1	1	0	1	0	1	0	1	0	0	0	0	0	0	0
0 1 0	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	0
0 1 1	0	1	1	0	0	1	0	1	0	1	1	0	0	0	0	0
1 0 0	0	1	1	0	0	1	0	1	1	0	0	0	0	0	0	0
1 1 0	0	1	1	0	1	0	1	0	0	1	0	0	0	0	0	0
1 1 1	1	1	0	0	0	1	1	0	1	1	0	0	0	0	0	0

Signal Source patterns to drive the Network are created with the Pattern Editor. This Editor allows the user to create his own pattern of 1's and 0's for each of 18 different sources for up to 256 clock times each. A variety of commands are available to create random, binary, clock set/reset and clock-time defined patterns.

The system also creates a Fan-Out Report listing the gate number and input pin number of every input driven by every gate.

The Simulation output is available on the CRT or on a printer. For CRT output up to 31 gate output states can be maintained. For printer output up to 70 output states can be monitored. A typical simulation output looks like this:

SIMULATION RUN

```
          NODES MONITORED
          00000000000000000000000000000000
  BIT     00000000011111111112222222223333
 TIME     12345678901234567890123456789012
 0        11100000000110000011000100100111
 1        01100111000011100111010110101111
 2        10101101010000100011010111111011
 3        00101010000101100011000100100111
 4        11001000011110000010010000101111
 5        01001101000110001011000100101111
 6        10001100000011100011110010101111
 7        00011000001000101010010010110111
 8        11100000000110000011100000110111
 9        01100111000011100111010110111111
 10       10101101010000100011010111111011
 11       00101010000101100011000100100111
 12       11001000011110000010010000101111
 13       01001101000110001011000100101111
 14       10001100100011100011110010101111
 15       00011000001000111010010010110111
 16       11100000000110010011100000110111
 17       01100111000011100111010110111111
 18       10101101010000100011010111111011
 19       00101010000101100011000100100111
 20       11001000011110000010010000101111
```

LOGIC DESIGNER AND SIMULATOR

AT A GLANCE

Simulation Type	Boolean State Analysis.
Input	Drawn Logic Diagram. Keyed-in Network Description. Signal Source and Patterns. Macro Truth Tables.
Output	CRT Logic Diagram (or Graphics dump to Printer). Gate Output 1-0 States vs Clock Time. Fanout Report. Input Pattern Listings. Macro Library. Network Listing.
Components Supported	NOR/OR, NAND/AND, Exclusive-OR, D FLIP FLOP, T FLIP FLOP, JK FLIP FLOP, 1 to 32 bit Shift Register, 16x3-variable Macros.
Maximum # of Gates	1000
Simulation Time (typical)	0.04 sec./gate/clock time (typically 15-30 min. per run).
Hardware Required	Apple II or II Plus/48K RAM. 2 Disk Drives DOS 3.3 80 Column Printer (optional). IBM PC with 128K RAM. Color Graphics Adaptor Board. Single Disk Drive. DOS 1.1 80 Column Printer (optional).
Medium Supplied In.	Supplied on a 5-1/4" mini floppy diskette with a 50 page instruction manual.
Product Price	$250.00
Manual and Demo Disk Package	$30.00 (Refundable towards product purchase).

Mathematics Series

If you're a student, teacher, mathematician, engineer or scientist in search of mathematical analysis routines, this package is for you. Elegantly written and user-oriented, this group of four programs makes maximal use of HI-Resolution plotting capabilities to augment math routines and display the results. The program contains a master menu to run any one of the following programs:

Statistical Analysis I: This is a general purpose menu-driven statistics package that allows the user to analyze numerical data bases. The program computes and displays:

- Mean
- Standard Deviation
- Frequency Distribution Plot
- Simple Linear Regression Line
- SLR Equation Co-efficient
- Data Points

Included are routines for disk data file I/O, editing and printer output.

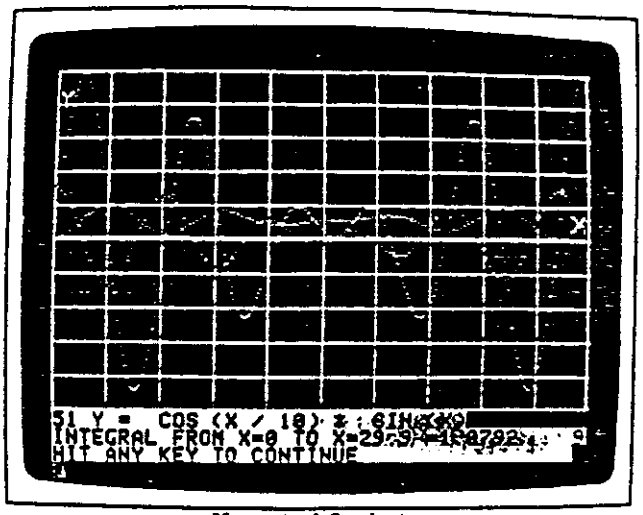
Numerical Analysis: This program will plot any two variable equations that you can write using standard Basic arithmetic functions. The program will plot the equation, its integral, and its derivative. It will determine and list roots, maxima or minima encountered and the integral value over the plot range.

Matrix: This program allows you to solve for the inverse, determinant and solution matrix for linear systems of up to 54 equations in 54 unknowns. It uses standard Gauss elimination with pivoting for maximum efficiency. Included are standard data base management routines for editing, disk I/O and printer reports of both data and results.

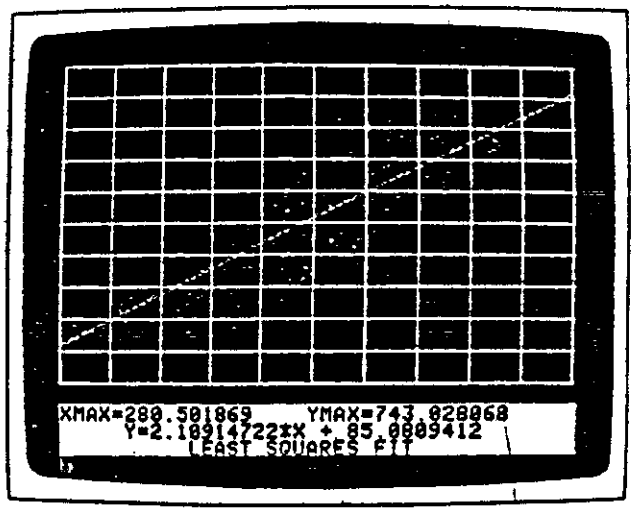
3D Surface Plotter: Ever wonder what a Black Hole's local field looks like? You can plot it in 3 dimensions with this program. This program does general purpose 3-D plotting of any 3 variable 3 variable equations that you can write using standard Basic arithmetic functions. It performs either hidden-line or transparent plots. Disk I/O routines are included for saving plot pictures on diskette.

The programs are all menu-driven and employ extensive prompting for ease of use. The entire series of programs is supplied on a single disk together with demos and an instruction manual. For

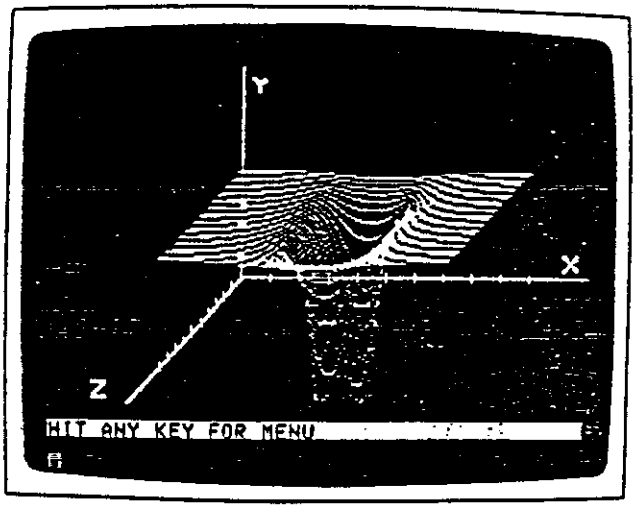
Order No.: AM-0001 **PRICE: $49.95**



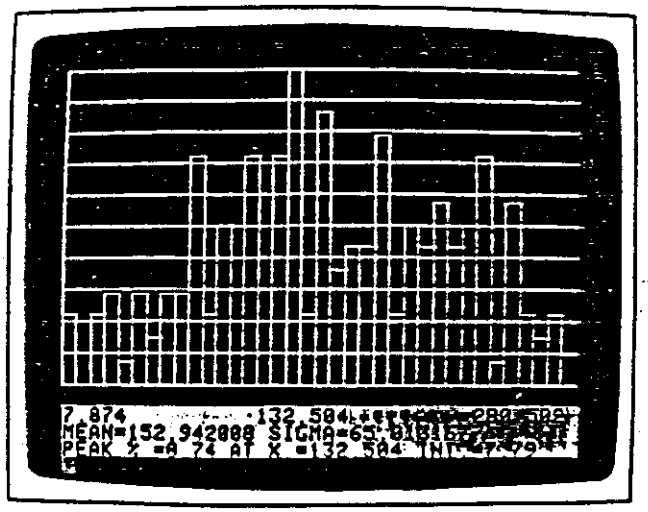
Numerical Analysis



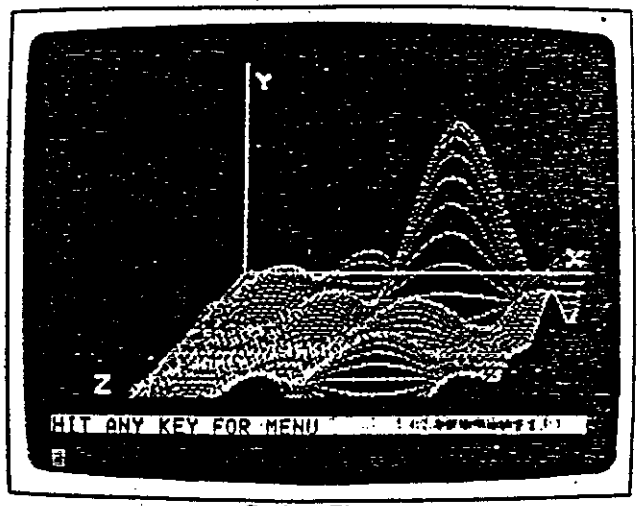
Statistical Analysis



Surface Plotter



Statistical Analysis



Surface Plotter